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# An Active Voltage Conditioner for Power Distribution Systems Using Hysterisis Controller

**Maamar Taleb**
*Department of Electrical and Electronics Engineering, University of Bahrain,*
*P.O. Box 32038, Isa Town, Bahrain*
*Email: maamar@eng.uob.bh*

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**Abstract.** This paper presents a model for an active voltage conditioner. This voltage conditioner is useful for power distribution systems in which power quality issue is of primary concern. The voltage conditioner consists a static var compensator (SVC ) and a series active voltage conditioner (AVC). The SVC type is a thyristor-controlled reactor (TCR). When using the SVC configuration individually, it is found that the rms value of load voltage is kept close to a desired/pre-set rms value, but unfortunately a considerate amount of harmonics is noted in the load voltage waveform. Computer simulations show that a 14.5% total harmonic distortion factor (THD) can be found in the load voltage waveform. Thus, an AVC is introduced in series with the SVC to take care of harmonics cancellation. The AVC is made of a single phase full wave bridge rectifier, a bridge inverter, and a series transformer. The bridge inverter is controlled by a simple hysterisis control circuit. When using the AVC in conjunction with the SVC, it showed the load voltage is kept near the desired rms value and no more than 0.98% total harmonic distortion factor (THD) is found its waveform. The performance of the SVC as well as the one of the AVC are obtained from MATLAB/SIMULINK computer simulation program.

***Keywords:*** Static voltage compensators, Active voltage conditioners, Power system harmonics, Power quality, MATLAB simulation, Electrical engineering education.

## Introduction

Static var compensators (SVC) have been applied to utility and industrial power for many years. Therefore, SVCs are not new to the industry, and by themselves, are not an overly complex device. To understand the need of installing an SVC when needed, consider the simple per-phase system equivalent circuit shown in Fig. 1(a) [1] by means of the ac system Thevenin equivalent, where the internal impedance of the ac system is assumed to be purely inductive. Figure 1(b) shows the phasor diagram for a lagging power factor load $P+jQ$ with a current $I=I_p+jI_q$, which lags the terminal voltage $V_t$. An increase $\Delta Q$ in the lagging vars drawn by the load causes the reactive current

component to increase to $I_q+\Delta I_q$, while $I_p$ is assumed to be unchanged. The phasor diagram for the increased $Q$ is indicated by "primed" quantities in Fig. 1(b) where the magnitude of the internal system voltage $V_s$ remains the same as before the change. The phasor diagram of Fig. 1(b) shows a drop in the terminal voltage by $\Delta V_t$ caused by an increase in the lagging reactive power drawn by the load. In this case, even if $I_p$ remains constant, the real power $P$ will decrease because of the reduction in $V_t$. For comparison purposes, Fig. 1(c) shows the phasor diagram where the percentage change in $I_p$ is the same as the percentage change in $I_q$ in Fig. 1(b), while $I_q$ is assumed to be unchanged. Figure 1(c) shows that the voltage change $\Delta V_t$ is small due to a change in $I_p$. The last observation suggests that for the sake of controlling the terminal voltage $V_t$, a reactive power source rather than a real power source should be installed in shunt with the load to compensate for any temporarily need of power by the load. This required source can be simply thought as a variable capacitor bank. Varying this capacitor should be fast and therefore it can not be done mechanically. To perform such a requirement, a fixed capacitor is installed in shunt with a controlled power semi-conductor switches in series with a fixed power inductor element, as shown in Fig. 2. Controlling the on/off switching times (turn-on and turn-off) of the semi-conductor switches will ultimately vary the reactive power needed by the system.

This paper investigates the performance of a SVC model of Fig. 2, referred in

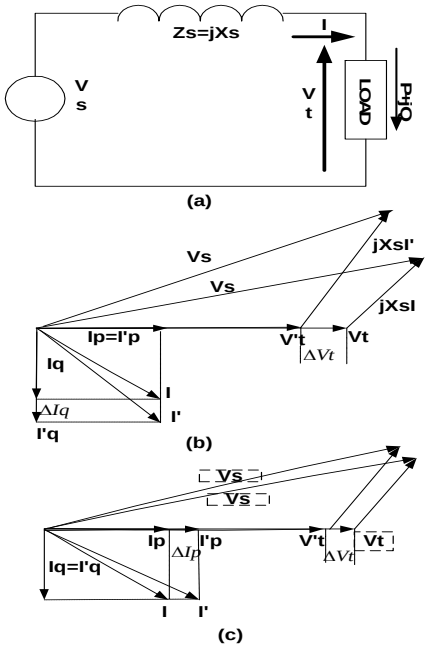



**Fig. 1. Effect of load on the terminal voltage: a) Equivalent cricuit. b) Change in real load current. c) Change in reactive load current.**

literature as a thyristor-controlled reactor (TCR type). The inductor of the TCR is controlled by two back-to-back thyristors.

The MATLAB computer simulations show the SVC/TCR performs its duty as intended. This duty consists of maintaining the rms load voltage near the desired value when the source voltage of figure varies between 300 to 330 V rms value. Unfortunately, under a number of operating conditions, a distorted waveform is encountered in the load voltage signal. Thus, an active voltage conditioner is suggested. Such conditioner is introduced between the SVC and the load. The duty of AVC consists of canceling the harmonics generated by the SVC. The AVC is made of a single phase full wave bridge rectifier, a bridge inverter, and a series transformer. The bridge inverter has four transistors of type IGBT and it is controlled by a simple hysterisis controller.

The performance of the SVC shows that a desired rms value of the SVC voltage is reached. More importantly, the load voltage has nearly null harmonic voltages. Both performances (i.e. SVC and AVC performances ) are tabulated using the computer toolbox: MATLAB/SIMULINK [2].

## Static Var Compensator Model and Performance

Figure 2 shows the general circuit diagram of the SVC as well as its main control blocks. The figure shows a voltage source in series with a series impedance. The impedance represents the source internal impedance plus the feeder impedance. The SVC configuration is shunted with a power load. The SVC contains a fixed capacitor in parallel with the thyristor controlled reactor (TCR). The control blocks represent actually the firing angle control circuit needed by the thyristors of the TCR branch.

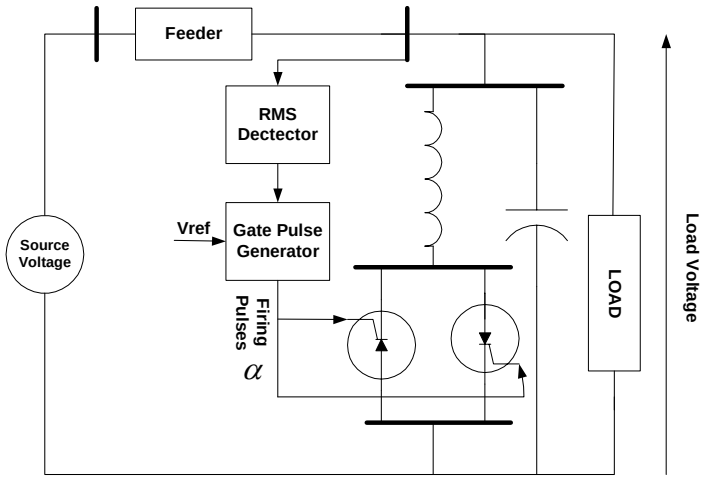



**Fig. 2. System investigated.**

The control blocks consist of:

1) A rms detector which measures simply the effective (rms) value of the load voltage or the SVC branch voltage.
2) A gate pulse generator (GPG) whose purpose is to compare first the SVC branch rms voltage with a reference voltage and based on this comparison, it initiates desired accurate instants of firing angle. Content detail of the gate pulse generator is shown in Fig. 3. This figure is actually a MATLAB/SIMULINK block diagram of the used firing angle control circuit. Input 1 (In1) reads the measured rms value of the load voltage. Input 2 (In2) takes instantaneous value of the load voltage. Output 1 (Out1) generates the pulses to the thyristors. Under a certain operating condition, the anticipated signals at some stages of Fig. 3 are depicted in Fig. 4.

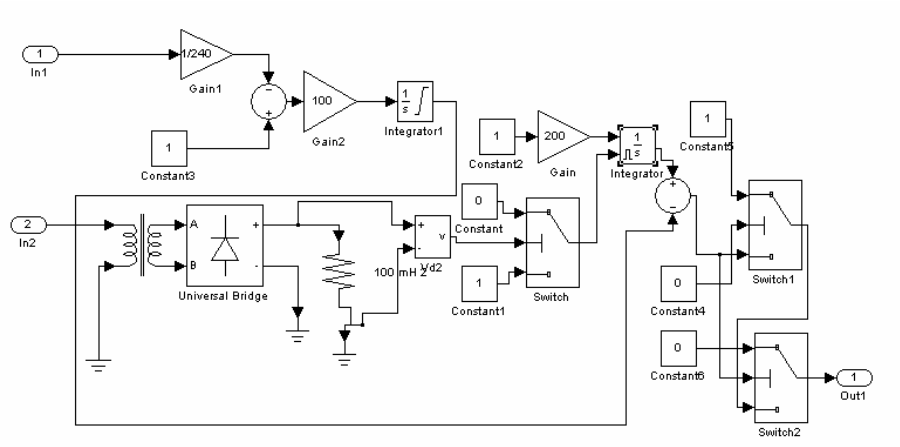



**Fig. 3. SVC firing angle control circuit.**

The values of the parameters of Fig. 2 are shown in Table 1.

**Table 1. Parameters values of Fig. 2**

| **50 Hz source voltage rms value** | **300 V to 330 V** | |
|---|---|---|
| Feeder | Resistance ( $\Omega$ ) | Inductance (mH) |
| | 1.16 | 9.8 |
| Load | Real power | Reactive power |
| | 7.5 kW | 4.647 Kvar |
| Static var compensator SVC | Fixed capacitor ( $\mu F$ ) | Inductor (mH) |
| | 225 | 1 |
| Reference voltage | 240 Volts | |

To predict the performance of the power system understudy, MATLAB computer simulations were done. Figure A-1 of the appendix represents the MATLAB/SIMULINK circuit diagram of Fig. 2. In the simulations, the source voltage was assumed to vary between 300 V and 330 V rms value. As it may be noted that the supply voltage is in the range of 300 V while the desired load voltage is 240 V. This means that the feeder has a high impedance. Actually, the considered system is thought to be a very weak system. Such system was witnessed in one country in North Africa. It was fluctuating weak system feeding certain 15 hp irrigation pumps. Figure 5 depicts two operating point results.

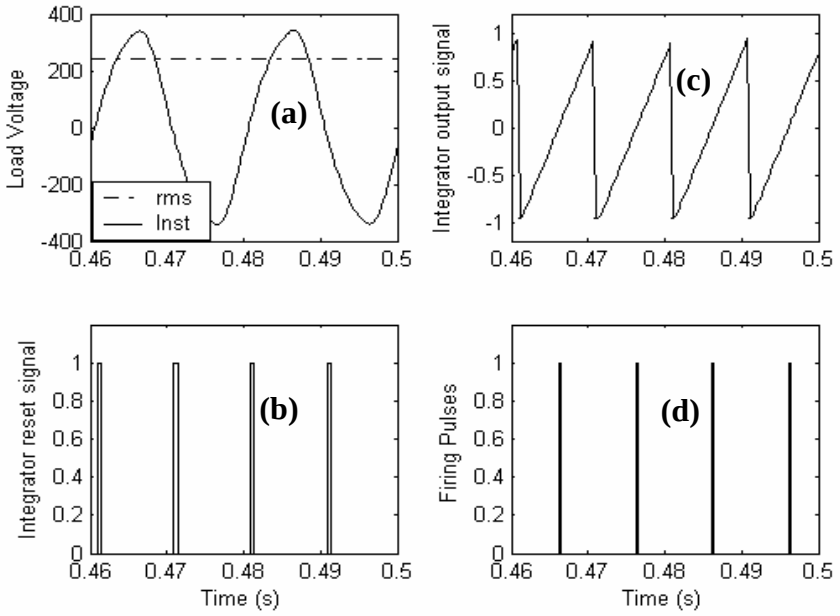



**Fig. 4. Some signals of SVC firing angle control circuit of Fig. 3: a) rms and Instantaneous load voltage. b) Integrator reset signal. c) Integrator output signal. d) Location of firing angle pulses.**

As it is observed from the solid curves of subfigures 5(b) and 5(f), the load voltage is kept or controlled to 240 V rms value under the two possible values of the source voltage. Therefore, the SVC is performing its intended task adequately. Note the level of the current in the TCR inductor. In the case of the 330 V, TCR current is badly needed to drop the voltage-down, whereas in the case of the 300 V voltage source, less TCR current is needed because of the need of load voltage compensation by the SVC fixed capacitor.

A careful glance at the load voltage waveform, one can deduce that the load voltage waveform is distorted. This distortion can be further aggravated if the system of Fig. 2 is

assumed to operate under other possible values of the source voltage. Figure 6(a) shows two waveforms of the load voltage. The solid one is obtained under a 312 V source voltage while the dashed one is obtained under a 330 V source voltage. The distortion in the load voltage is due of course to the non-linearity of the TCR current.

Actually, this non-linearity is not a new thing to discover. It has been already documented in the literature [3]. This non-linearity creates harmonics that are spread to the power systems components and affects their desired performances, in particular if the load close to the SVC bus is sensitive or vulnerable to harmonics. To get an idea about how much harmonics are present in the load voltage waveform, the total harmonic distortion factor (THD) is computed under the possible range of rms source voltage variations. Figure 6(b) depicts the value of such THD. As it is seen, almost 14.5% is noted when the source voltage is 312 V.

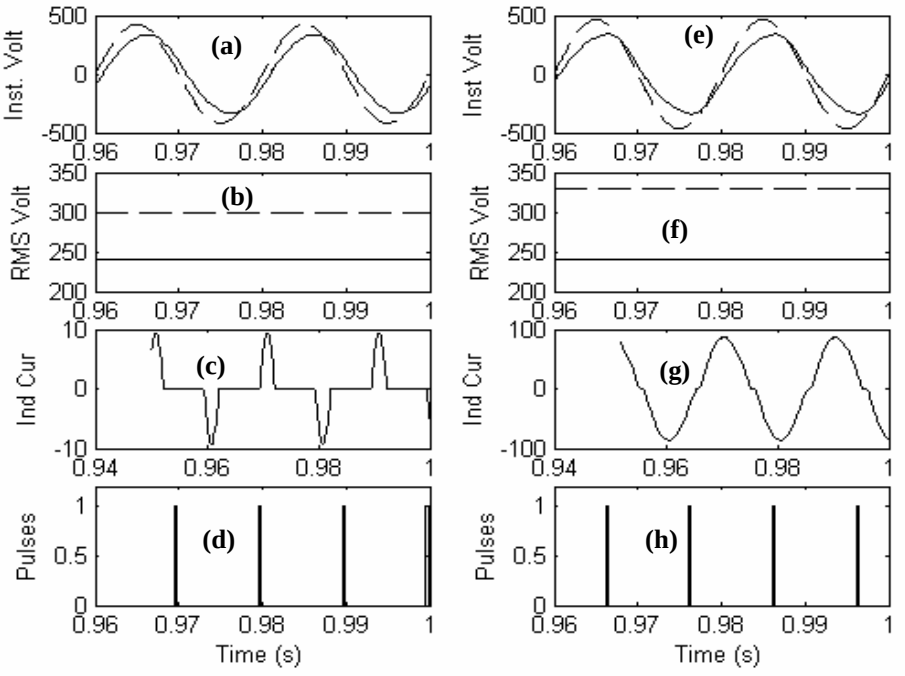



**Fig. 5. SVC Performance:** ***Left Column:*** **Results under 300V source voltage: a) Instantaneous source and load voltage. b) rms source and load voltage. c) TCR current. d) Firing angle positions.** ***Right Column:*** **Results under 330V source voltage: e) Instantaneous source and load voltage. f) rms source and load voltage. g) TCR current. h) Firing angle positions.**

Therefore, at the expense of guarantying a constant rms value for the load voltage, harmonic voltages are generated by the SVC configuration/module. Thus, remedies should be considered with the intention of taking care of the unwanted generated

harmonic voltages. This is the duty of the active voltage conditioner that is treated in the following section.

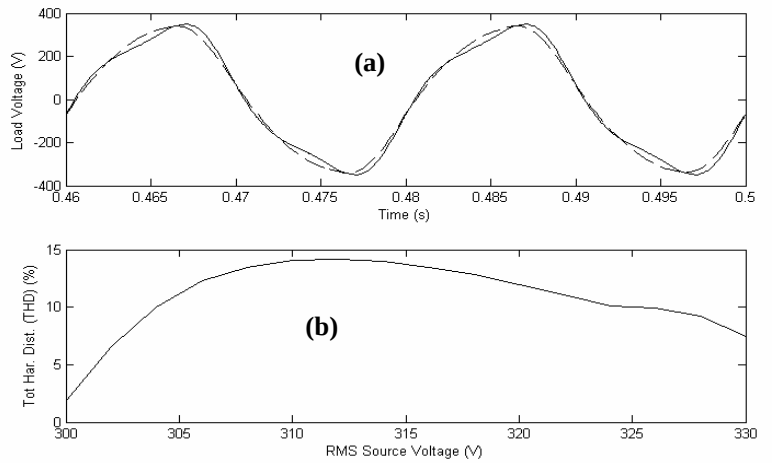



**Fig. 6. SVC performance: a) Instantaneous load voltage when source voltage is 312 and 330 V respectively. b) Total harmonic distortion factor (THD) when source voltage is varied between 300 to 330 V in a step of 2V each time.**

## Static Var Compensator and Active Voltage Conditioner Model and Performance

The presence of distortion in the load voltage waveform may affect power apparatuses performance drastically [4-5]. This distortion can be acceptable or tolerable up to a certain level [6-7]. Therefore, power harmonic filters need to be installed and that is to remove or control the level of the harmonic distortion. The power harmonic filters might be either passive or active. The active voltage conditioner is one of the active power filters. References [9-16] document the principle of operation and uses of the active power filters. The ideology of the active voltage conditioner used in this paper is originally suggested in reference [9]. What is different between the active filter of reference [9] and the active voltage conditioner of this paper is the type of controller.

Figure 7 shows the layout and location of the active voltage conditioner in the system under investigation. The active voltage conditioner consists of a rectifier, an inverter a power transformer and some control blocks.

- The rectifier is a simple full wave diode bridge.
- The inverter is made of four insulated gate base transistors ( i.e. IGBT transistors).
- The primary winding of transformer is connected across the output terminals of a full wave bridge inverter while the secondary winding has one terminal connected to the bus having the distorted waveform supply voltage (i.e. SVC bus) and the other terminal connected to the load.

- The control blocks consist of two cascade blocks. Block 1, termed harmonic voltage detector whose duty is to detect the harmonic voltages content in the SVC bus voltage waveform. Block 2, termed hysterisis controller, takes the output of the previous harmonic voltage detector as a reference signal and generates the driving signals to the gates of the inverter bridge made of four IGBT transistors. This should be fulfilled in a way that the voltage across the output terminals of the transformer (i.e. transformer secondary winding terminals) should follow the desired signal assessed by the harmonic voltage detector block.

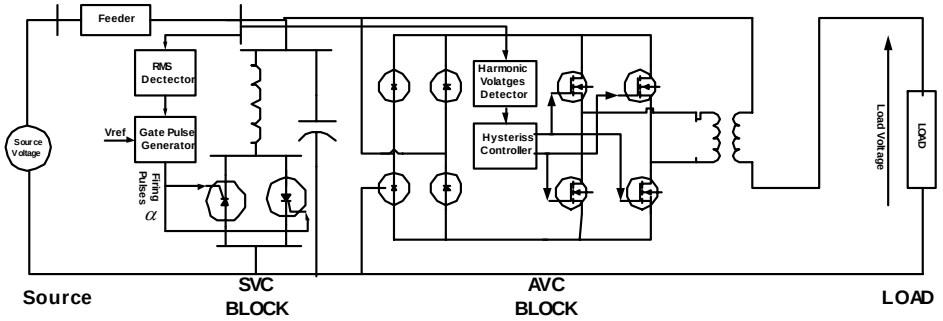



**Fig. 7. System investigated: SVC and AVC configuration.**

Figure 8 shows the contents of the AVC control blocks. Figure 8(a) is the harmonic voltage detector. Its principle of operation is as follows: The SVC bus voltage waveform is supplied to input 1 (In1 port). Input 1 signal is fed to a discrete Fourier transform (DFT) block. The DFT output provides the magnitude and phase angle (in radian) of the fundamental component of the SVC bus load voltage. Instantaneous value of the fundamental component is obtained at the output of function f(u) block. Subtracting the output of f(u) block from input 1 signal results in a signal containing the harmonic voltages that are embedded in the SVC bus voltage. This is the signal of the output (Out1 port).

Figure 8(b) is the hysterisis controller. This controller has three inputs. One input (port In2) is connected to the output of the harmonic voltage detector (port Out1). The second input (port In3) is the load bus voltage. The third input (port In4) is connected to the ground. Subtracting the load bus voltage from the harmonic voltage detector output gives an error signal that is fed to a hysterisis controller (i.e. the relay block). The duty of the relay block consists of either changing the status of the relay output port whenever the level of error signal is outside specified hysterisis limits (i.e. allowable hysterisis band), or keeping the relay output signal intact if the input error signal is within specified hysterisis limits. The relay output is fed to a switch block. The switch block plays the role of comparator. The switch provides a high state when the input is higher than a certain threshold value and a low state when the input is less than that threshold value. The switch decision will be found at port Out2 of Fig. 8(b). Port Out3 takes the complementary value of port Out2 output. That is, if Out3 status is high then Out2 status

is low, and vice versa if Out3 status is low then Out2 status is high. Out2 and Out3 are connected to the gates of IGBT transistors of the bridge inverter as shown in Fig. A-2.

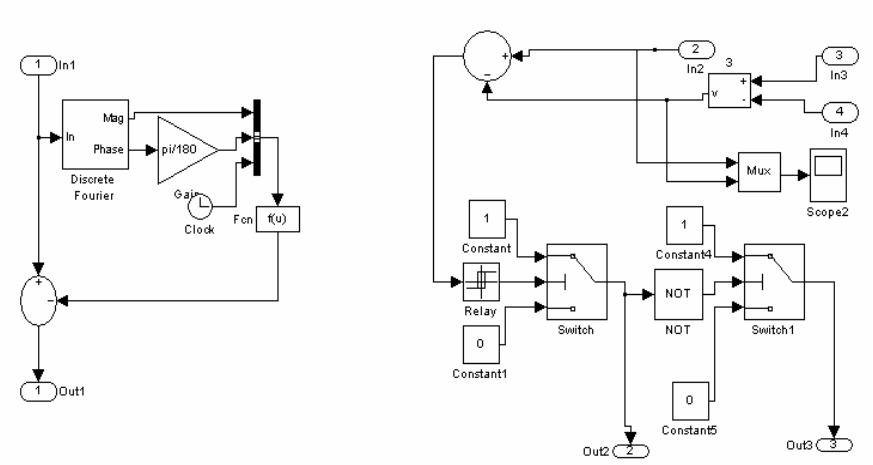



**Fig. 8: Control blocks of the active voltage conditioner: a) Harmonic voltage detector. b) Hysterisis controller.**

Figure A-2 in the appendix is the MATLAB/SIMULINK circuit diagram of Fig. 7. For the sake of clarity, Fig. A-2 is split into two parts. Part A-2(a) contains the main source and the SVC branch associated with its control blocks, while Part A-2(b) contains the AVC with its control block and the constant power load.

In order to test the performance of the power system of Fig. A-2, the source voltage has been pretended to vary between 300 V and 330 V rms value. Figure 9 depicts two operating point MATLAB/SIMULINK simulation results. The left column results are obtained when the source voltage is 312 V rms value. The right column results are obtained when the source voltage is 330 V rms value. The instantaneous and rms values of the source voltage are shown in subfigures 9(a) and 9(d) respectively. Of course, the rms value is 312 V in subfigure 9(a) and it is 330 V in the case of subfigure 9(d) (i.e. dashed lines). Subfigures 9(b) and 9(e) visualize three curves. The three curves represent actually the SVC bus instantaneous voltage (dashed line), the load instantaneous voltage (solid line), and the SVC bus rms voltage (dashed line). It is quite clear that the SVC is guarantying the 240 v rms value in the two pretended operating source voltages. But unfortunately, the SVC voltage waveform is distorted. Such distortion is alleviated by the AVC which provides nearly a pure sinusoidal voltage across the load terminals. This observation is noted under both operating source voltage conditions (i.e. 312 V and 330 V source voltage conditions). Thus, it can be concluded from the simulation results that the AVC is fulfilling its targeted task accurately. The total harmonic distortion factor (THD) is computed for both operating

conditions. It is found to not be exceeding a 0.98% value. Subfigures 9(c) and 9(f) depict the unwanted harmonic voltages signal and they appear across the secondary winding terminals of the AVC transformer. Note the hysterisis phenomena in both cases and it is clear to reconfirm that the AVC controller is performing its job neatly. Another remark that may be noted by the reader is that the amount or level of harmonic voltages in the SVC bus voltage in the case of the 330 V source voltage is less than its corresponding one in the case of 312 V source voltage.

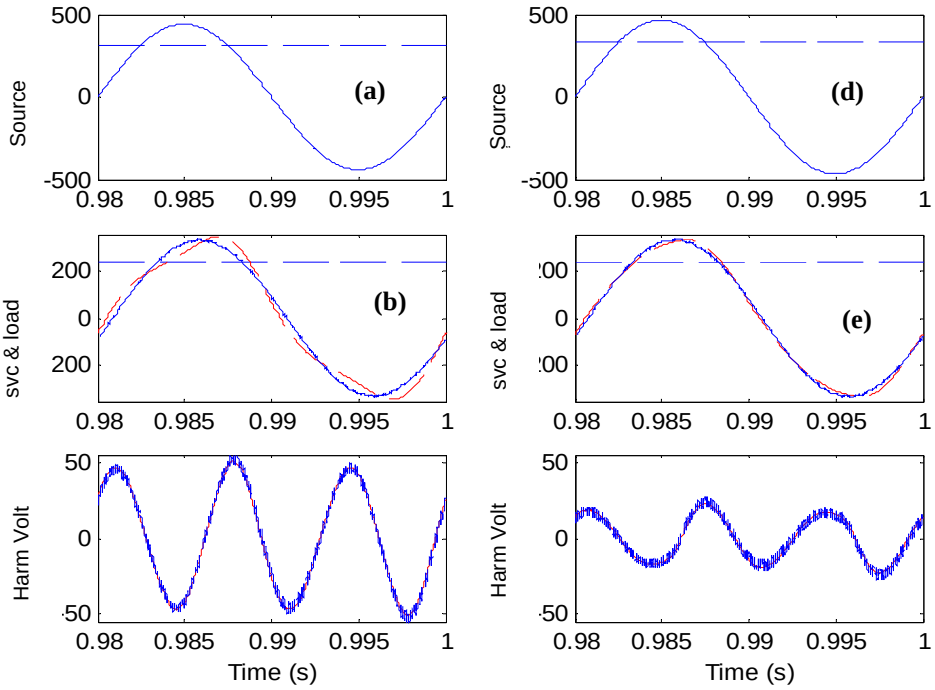



**Fig. 9. SVC and AVC performance: *Left Column*: Results under 312V source voltage: a) Instantaneous and rms source voltage. b) Instantaneous, rms SVC and Instantaneous load voltages. c) Voltage across the secondary winding terminals of the AVC transformer. *Right Column*: Results under 330V source voltage: d) Instantaneous and rms source voltage. e) Instantaneous, rms SVC and instantaneous load voltages. f) Voltage across the secondary winding terminals of the AVC transformer.**

This remark is obvious because the current in the TCR inductor is nearly sinusoidal (i.e. as shown earlier in subfigure 5(g)) in the case of the 330 V source voltage and consequently less harmonic voltages should be present in the SVC bus voltage. Figure 10 is no more than a magnification of subfigure 9(b). It is brought here for the sake of reclaiming that the SVC is guarantying a desired 240 V rms voltage value (horizontal dashed curves) and it is not caring about the quality of the SVC

voltage waveform. The introduction of the AVC in cascade with the SVC is providing a near pure sinusoidal voltage waveform (i.e. solid line).

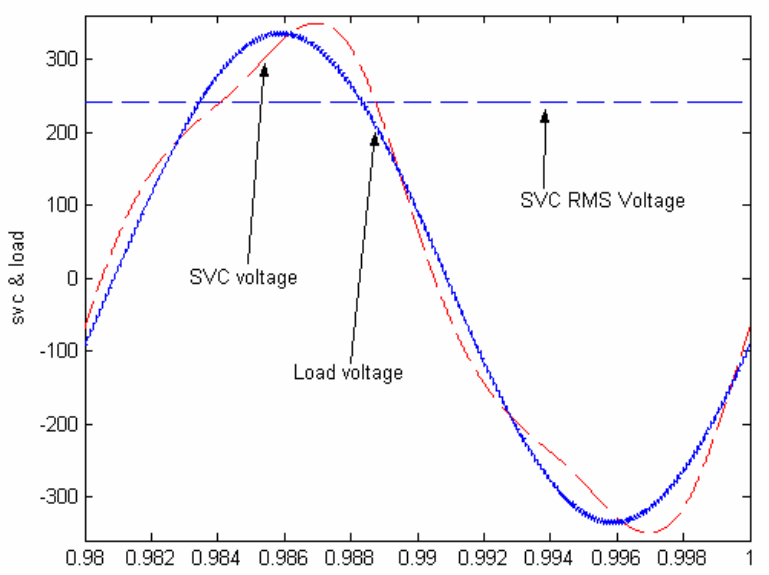



**Fig. 10. SVC and AVC performance: Instantaneous SVC voltage, rms SVC voltage and instantaneous load voltage.**

## Conclusion

In weak power distribution systems and when power quality is of primary concern, reactive power control seems to be a necessary measure to control load voltage. This can be done through the implementation of the static voltage compensator (SVC) of TCR type in conjunction with the active voltage conditioner (AVC). The performance of the AVC can be monitored/controlled by a proposed simple hysterisis controller. The characteristic of the proposed controller used in the AVC configuration persists in its simplicity when compared to other conventional controllers.

The SVC guaranties a desired rms voltage while the AVC guaranties the quality of the voltage waveform. Computer simulations in this paper show that when using only the SVC, the load voltage is controlled near a desired rms voltage value but a distorted SVC voltage waveform is encountered. However, when adding or attaching the AVC to the previous SVC, the simulations show that a quantitative as well as qualitative load voltage is reached regardless the voltage fluctuations that may occur often in the source voltage.

The author admits that the SVCs are usually used for medium voltages. But, here it has been applied to low voltage. The work performed here can be also extended to medium voltage ranges.

## References


[1] Mohan, N., Undland, T.M. and Robbins, W.P. *Power Electronics: Converters, Applications, and Design*. 2nd ed., New York: John Wiley and Sons Inc., 1995.

[2] MATLAB, Version 6.5.018091 Release 13, copyright 1984-2002, The Math Works Incorporation, 2002.

[3] Yacamini, R. and Resende, J.W. "Harmonic Generation by HVDC Schemes Involving Converters and Static VAr Compensators." *IEE Proceedings: Generation, Transmission and Distribution*, 143, No. 1 (January 1996), 66–74.

[4] Hui, S.Y.R. "A Brief Review of the Effects and Control of Harmonics in Supply Systems and Machines Drives." *Journal of Electrical and Electronics Engineering, Australia, IE Aust. & IREE Aust*., 13, No. 6, (1993), 23-41.

[5] Barros, J. and Diego, R.I. "Effects of Non-sinusoidal Supply on the Voltage Tolerance of Equipment." *IEEE Power Engineering Review*, 22 (July 2002), 46-47.

[6] IEEE Recommended Practice for Monitoring Electric Power Quality, IEEE Std 1159-1995, New Jersey.

[7] Jackson, G.A. "Setting the Standards: The European EMC Directive." *IEE Review*, 36, No. 4 (1990), 460-465.

[8] "Australian Standard AS 2279." Parts 1-4, 1991.

[9] Ezer, D., Hanna, R.A. and Penny, J. "Active Voltage Correction for Industrial Plants." *IEEE Trans. on Industry Applications*, 38 (Nov./Dec. 2002), 1641-1646.

[10] Jou, H.L., Wu, J.C., Wu, K.D., Tsai, C. and Kuo, Y.T. "A New Control Algorithm of Active Power Line Conditioner for Improving Power Quality." *Electric Power Systems Research*, 70, No. 1 (June 2004), 1-6.

[11] Jou, H.L. and Wu, J.C. "Performance Comparison of Single-phase Active Power Line Conditioners for Harmonic Suppression and Reactive Power Compensation." *Electric Power Systems Research*, 31, No. 2 (November 1994), 137-145.

[12] Wu, J.C. and Jou, H.L. "A New Power Conditioning Strategy." *Electric Power Systems Research*, 29, No. 3 (May 1994), 217-226.

[13] Claro, C.A. and Campos, A. "Analysis and Design of a Series AC Voltage Conditioner Employing a Dead Beat Control Technique." *Industrial Electronics Society, 1998. IECON '98. Proceedings of the 24th Annual Conference of the IEEE*, 1 (31 Aug.-4 Sept. 1998), 385- 390.

[14] Barros, J. "Discussion of Active Voltage Correction for Industrial Plants." *IEEE Transactions on Industry Applications*, 39, No. 4 (July-Aug. 2003), 1211-1218.

[15] Watanabe, E.H. and Aredes, M. "Power Quality Considerations on Shunt/Series Current and Voltage Conditioners." *10th International Conference on Harmonics and Quality of Power 2002*, 2 (2002), 595 – 600.

[16] Nunez, C., Cardenas, V., Alarcon, G. and Oliver, M. "Voltage Disturbances and Unbalance Compensation by the Use of a 3-phase Series Active Filter." *IEEE 32nd Annual Power Electronics Specialists Conference 2001 (PESC 2001)*, 2, (17-21 June 2001), 571–576.

## Appendix

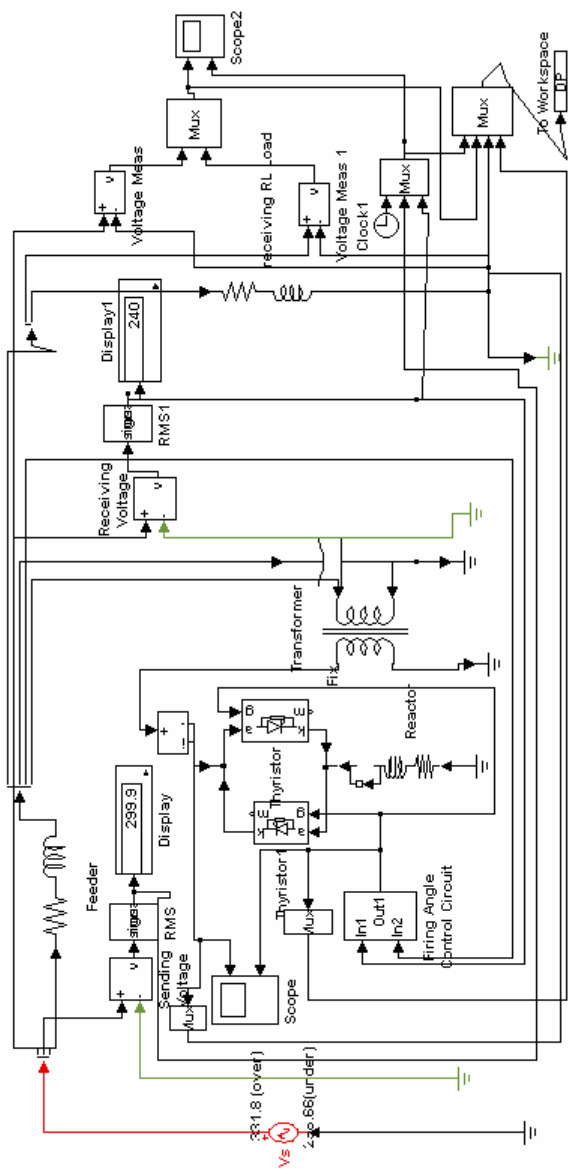
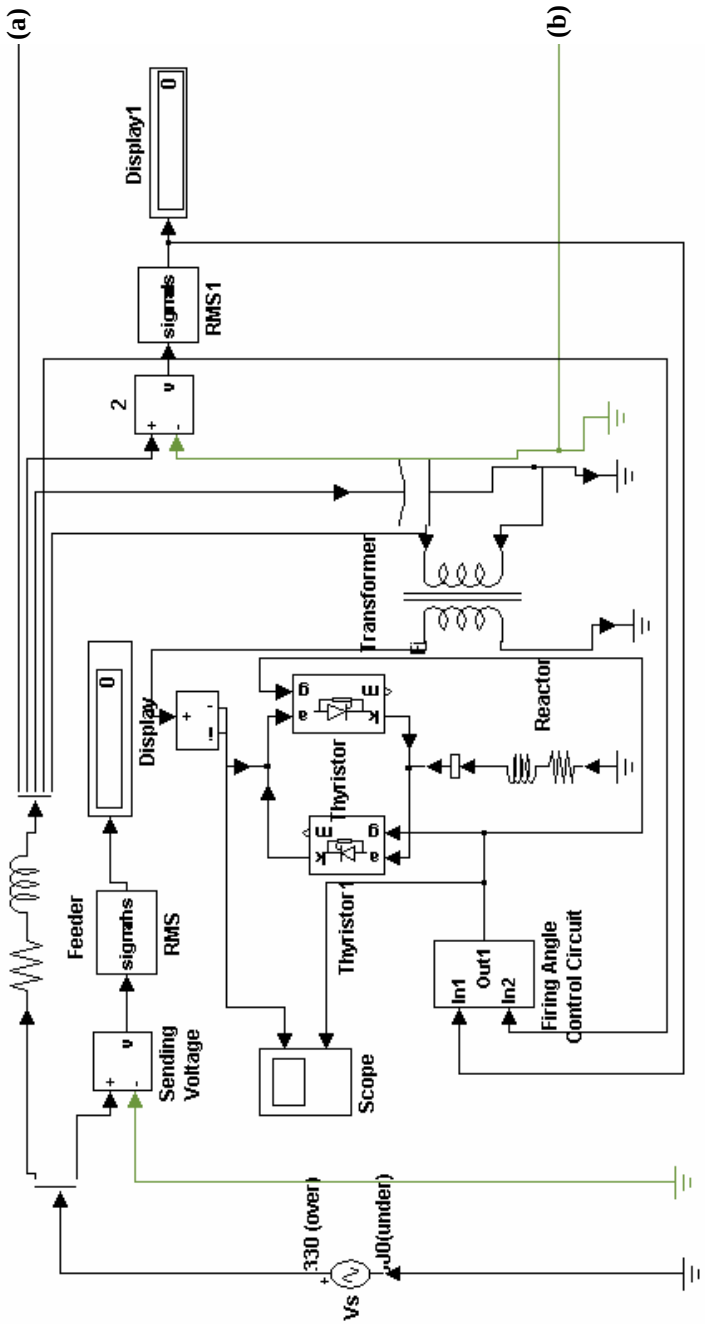



**Fig. A.1: SIMULINK model of the SVC. The content of the firing angle control circuit block is the one shown in Fig. 3.**




(a)

**Fig. A.2: SIMULINK model of the SVC and the AVC. The content of the firing angle control circuit block is the one shown in Fig. 3.**

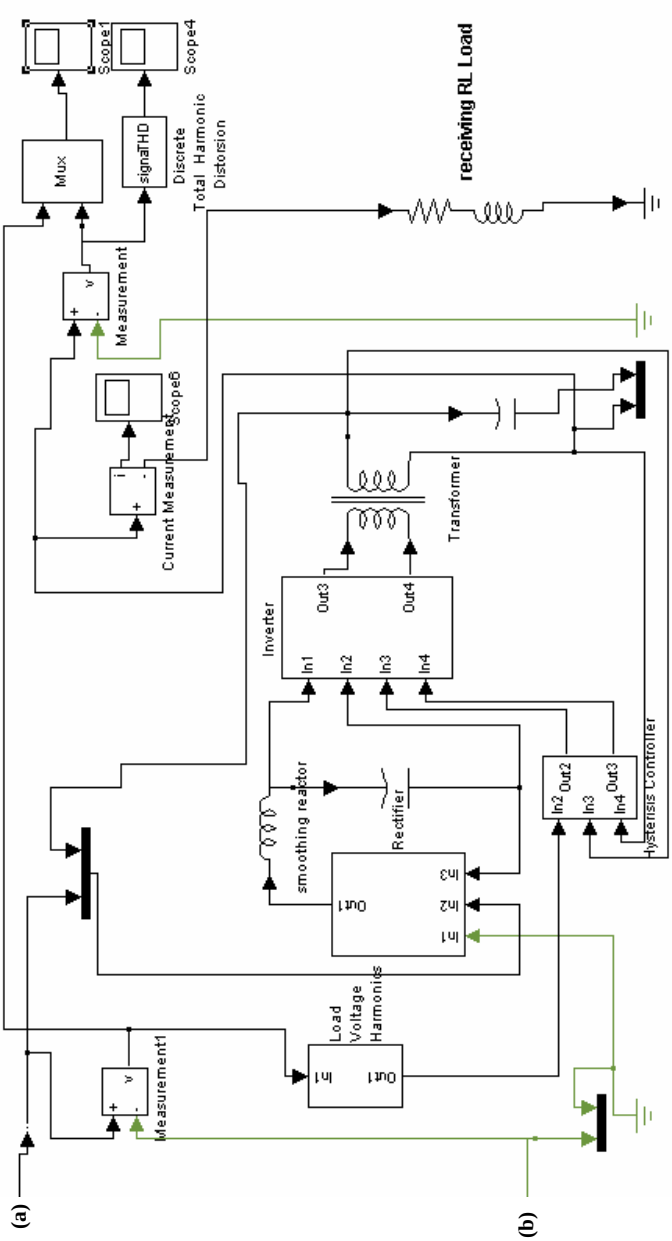



**Fig. A.2: SIMULINK model of the SVC and the AVC. The content of the load voltage harmonics and hysterisis controller blocks are the ones shown in Fig. 8(a) and 8(b) respectively.**

# مكيف فولطية فعال لأنظمة التوزيعات الكهربائية باستخدام محكم هيستريزس

**معمر طالب**

*جامعة البحرين*

*قسم الهندسة الكهربائية و الإلكترونية*

*ص.ب. ٣٢٠٣٨، مدينة عيسى*

*مملكة البحرين*

*البريد الإلكتروني:* maamar@eng.uob.bh

( قدِّم في ٢٠٠٥/٠٥/٢٢م، وقبل للنشر في ٢٠٠٦/٠١/٣٠م )

**ملخص البحث.** تقدم هذه الورقة نموذجًا لمكيف فولطية فعال يمكن استخدامه في أنظمة التوزيعات الكهربائية التي تكون فيها قضية نوعية القوى من الاهتمامات الأولى للمستهلك.

يتكون النموذج المقترح من معوض ثابت للفارات (SVC) ومكيف فولطية فعال (AVC). تبين الدراسة المقترحة أن استخدام المعوض الثابت للفارات بمفرده يضمن الحصول على القيمة المجدية المرغوبة فيها للفولطية على الحمل، ولكن للأسف ينتج مع هذا الضمان تشوه في شكل الفولطية المتواجدة على الحمل السابق. في هذا الصدد تبين المحاكات الحاسوبية أن المعامل الكلي للتشوه قد يقارب قيمة ١٤,٥٪ تحت ظروف تشغيل معينة. ولإلغاء مفعول التشوه الملحوظ تم إدخال مكيف فولطية فعال على التسلسل مع المعوض الثابت للفارات السابقة. يشتغل مكيف الفولطية الفعال بتوجيه وإشراف محكم الهيستريزس (Hysteresis Controller).

أثبت استخدام المعوض الثابت للفارات ومكيف الفولطية الفعال التحكم في القيمة المرغوبة للفولطية على الحمل وتقليص التشوه في شكلها المتواجد على الحمل، وبالتحديد لوحظ أن المعامل الكلي للتشوه قد تقلص إلى قيمة ٠,٩٨٪ بعدما أن كان ١٤,٥٪ كما ذكر آنفًا. يجدر بالذكر أن أداء المعوض الثابت للفارات ومكيف الفولطية الفعال قد قدر باستخدام برنامج MATLAB/SIMULINK.