J. King Saud Univ., Vol. (14), *Eng. Sci.* (2), pp.-211-219, Riyadh (A.H. 1422/2002)

Substrate Temperature Options for CSS Grown CdTe Polycrystalline Film Structures

A.R.M. Alamoud
Electrical Engineering Department, College of Engineering
King Saud University, P.O. Box 800, Riyadh 11421, Saudi Arabia

(Received 25 July, 2000; accepted for publication 23 May, 2001)

Abstract: Close-spaced sublimation (CSS) grown Cadmium Telluride (CdTe) thin films were characterized by deep level transient spectroscopy (DLTS), scanning electron microscopy (SEM), and photoluminescence (PL). The effect of substrate temperature variations on the device performance and interface and bulk properties was observed.

Introduction

Substantial progress has occurred in polycrystalline thin-film solar cells in the past decade. The main emphasis, though, is on CIS and CdTe types [1-4]. CdTe, owing to its excellent physical properties: high optical absorption coefficient, an ideal direct bandgap, and electrical properties that are relatively independent of the grain size, coupled with the relative ease of deposition by a wide variety of techniques, is poised to become a leading candidate for solar cell fabrication. Close-spaced sublimation fabrication technique is rapidly emerging as one of the most promising choices for thin-film, polycrystalline CdTe/CdS solar cells photovoltaic applications due to its relative simplicity, lower cost, and ease of scaling-up [5-9].

In this paper, the effect of substrate temperature variation on the CdS/CdTe device performance prepared by the close-spaced sublimation method (CSS) will be presented. Different techniques were used to characterize the CdS/CdTe bulk and interface properties and surface morphology and composition. These techniques include Deep Level Transient Spectroscopy (DLTS), Photoluminescence (PL), and Scanning Electron Microscopy (SEM).

Experimental

The Cadmium Sulfide (CdS) films were chemically grown, by the chemical bath deposition (CBD) method, on SnO_2 coated (0.4μm) glass substrates (corning 7059) by the reaction of $CdSO_4$ and thiourea (NH_2CSNH_2) in an aqueous solution [10,11]. The CdS films were grown to a thickness of 800-1000Å. The CdS surface was treated by dipping in a 1:40 HCl:DI water solution for about 10 seconds followed by annealing at 400°C in H_2 at 30 Torr for about 15 minutes.

The Cadmium Telluride (CdTe) thin films were deposited by the close-spaced sublimation method to a thickness of 7 µm. The deposition was carried out at a source temperature of 650°C and a substrate temperatures of 625°C, 600°C, 525°C, and 500°C in an ambient pressure of 14.5 He and 0.5 O_2 for five minutes [12,13]. These are referred to as sample #07C, #09C, #17C, and #19C respectively. Post-deposition treatment was carried out by dipping the CdTe films in a saturated solution of $CdCl_2$ in methanol. The $CdCl_2$ treatment was followed by a heat treatment for 30 minutes at 400 °C in a tube furnace. Finally, an HgTe contact was applied to the CdS/CdTe structure. Details of the CSS process and experimental setup can be found in the literature [14].

Results and Discussion

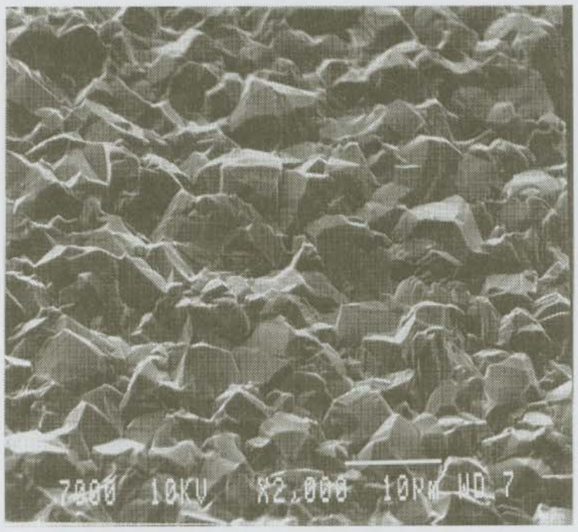
The measured parameters for the four CdS/CdTe structures are listed in Table 1. Device 07°C possesses the best performance of the group with an efficiency of about 12 percent. Open-circuit voltage values were found to increase with increasing substrate temperature. Table 1 shows that V_{oc} values improve with increasing substrate temperature until a substrate temperature of 600°C is reached. A large jump in V_{oc} takes place between substrate temperature values of 525°C and 600°C. This indicates that the substrate temperature for CdTe film growth should not be less than 600°C for an optimum device performance. The device V_{oc} reaches an optimum value at a substrate temperature between 600°C and 625°C. This is evident because V_{oc} of sample #07C (T_s= 625°C) is lower than V_{oc} of sample 09C (T_s= 600°C). It is believed, however, that the optimum substrate temperature is about 610°C. This has been shown to be true through the use of the "two-wave" temperature profile as opposed to the "conventional" constant temperature profile [15]. Sample #07C is, though, superior to other samples in the batch, including #09C, when it comes to efficiency η and short-circuit current I_{sc} values.

Table 1. Measured parameters of CdS/CdTe structures

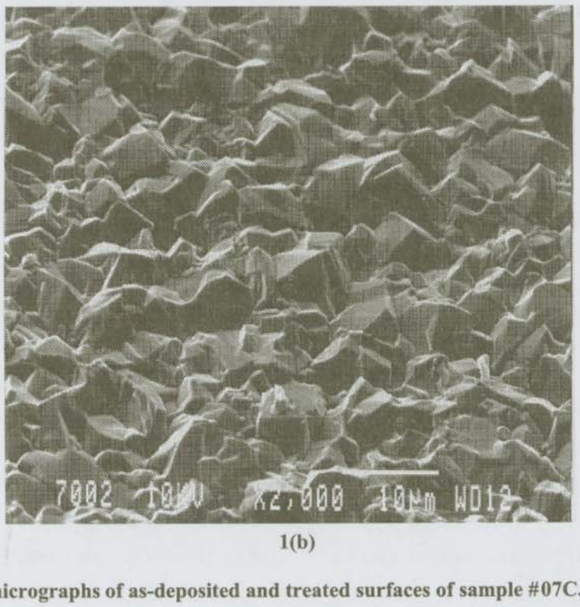
Sample #	T_s (°C)	V_{oc} (volt)	J_{sc} (mA/cm^2)	V_{mp} (volt)	J_{mp} (mA/cm^2)	FF (%)	η (%)
07C	625	0.76	23.52	0.59	20.27	66.7	11.96
09C	600	0.77	22.77	0.60	19.37	66.6	11.62
17C	525	0.71	18.43	0.51	15.48	60.3	7.89
19C	500	0.70	19.59	0.51	16.90	62.8	8.62

Scanning electron microscopy (SEM) analysis

Scanning Electron Microscopy (SEM) was used to study the effect of varying the substrate temperature on the morphology of the CdTe films grown by the close-spaced sublimation technique [13,14]. Figures 1a and 1b show SEM micrographs of the as deposited and the $CdCl_2$ treated CdS/CdTe structure surfaces, of sample #07C respectively. One can hardly see a difference between the two micrographs. That is to say, no grain growth has resulted from $CdCl_2$ treatment. This is due to the fact that the high substrate temperature (625°C in this case) during CdTe evaporation passivates the film surface making the $CdCl_2$ treatment essentially ineffective.



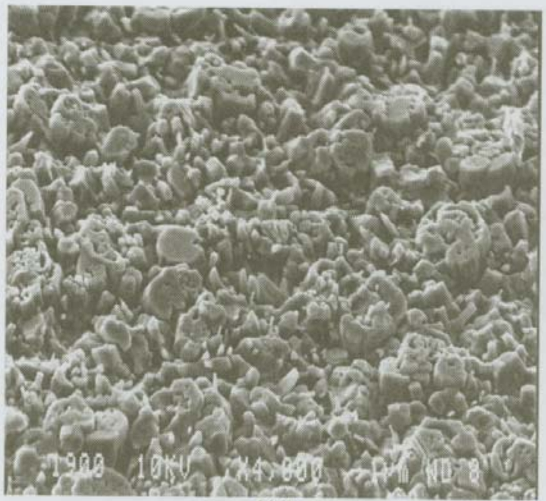
1(a)



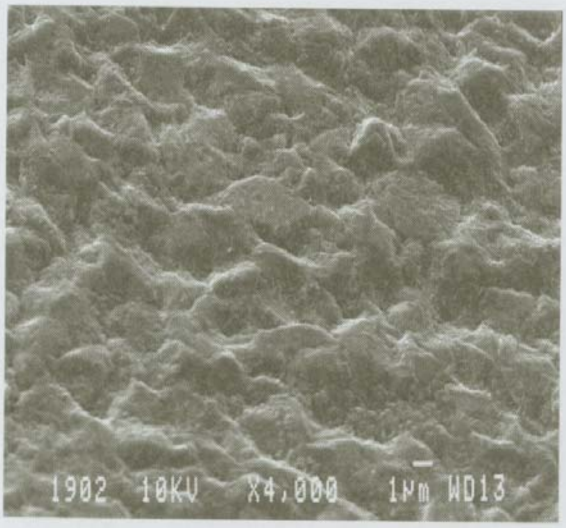
1(b)

Fig. 1 (a,b). SEM micrographs of as-deposited and treated surfaces of sample #07C.

On the other hand, a big difference is evident in condition of the as deposited (SEM micrograph of Fig. 2a) and treated (SEM micrograph of Figure 2b) surfaces of sample # 19C. The CdTe film of this sample was grown at a substrate temperature of 500°C. The effect of $CdCl_2$ treatment, in this case, is to increase the grain size as expected. A similar effect exists for sample #17C (T_s= 550°C) and sample #09C (T_s= 600°C). Comparing Figs. 1 and 2, one can see that the effect of $CdCl_2$ treatment decreases as the substrate temperature increases.



1(a)



2(b)

Fig. 2 (a,b). SEM micrographs of as-deposited and treated surfaces of sample #19C.

The SEM micrographs analysis for all samples revealed that the average grain size of the as deposited CdTe films is highly affected by the substrate temperature. It was found that the grain size of the as deposited CdTe films increases nonlinearly with the substrate temperature following a simple power series form. The SEM micrographs also show that the CdTe films of the above samples are free of voids or any other discontinuities and have a well-faceted grain structure.

Photoluminescence (PL) measurements

Photoluminescence measurements were performed on the front side (CdS/CdTe interface) and the back side (CdTe surface) of the four structures to study the defects (shallow) produced by the effect of the different substrate temperatures [18]. A He-Ne laser with a laser line at 632.8nm and an optimal power output of about 35mW was used. Results of PL measurements performed at 5K on the CdTe film (back of the structure) indicate that the quality of the CdTe film improves with increasing growth temperature resulting in a decrease of pinhole density. Sample #07C yielded the strongest near-band-edge (NBE) peak (see Figs. 3 and 4) indicating a relatively fewer deep traps and also the highest deep-level band (DLB) peak, indicating a low density of nonradiative recombination centers. Moreover, the ratio of the DLB peak to the NBE peak is only 0.26 compared to a value 1.18 for sample #19C (T_s=500°C).

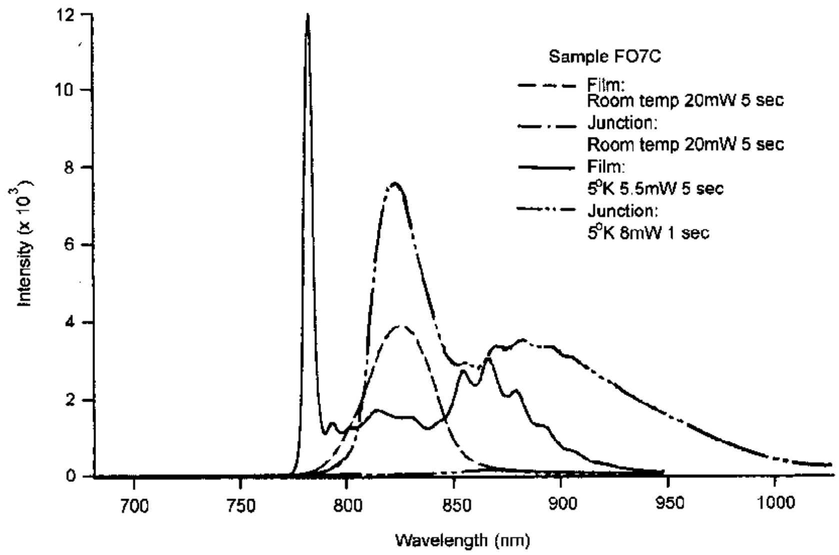


Fig. 3 PL Spectra of sample #07C.

PL spectra obtained from the CdS/CdTe interface at 5K for the four samples (see Fig. 4) reveal that the near band edge peak increases both in intensity and width with increasing growth temperature of the CdTe film. This would imply that the number of deep level traps decreases as the film growth temperature is increased. Moreover, a reduction of the B-B (exitons) peaks with increasing CdTe film substrate temperature is also observed. The NBE peak is located at 823 nm while the DLB peak is located at about 888 nm. Both NBE and DLB peaks shift towards the infrared region with increasing substrate temperature.

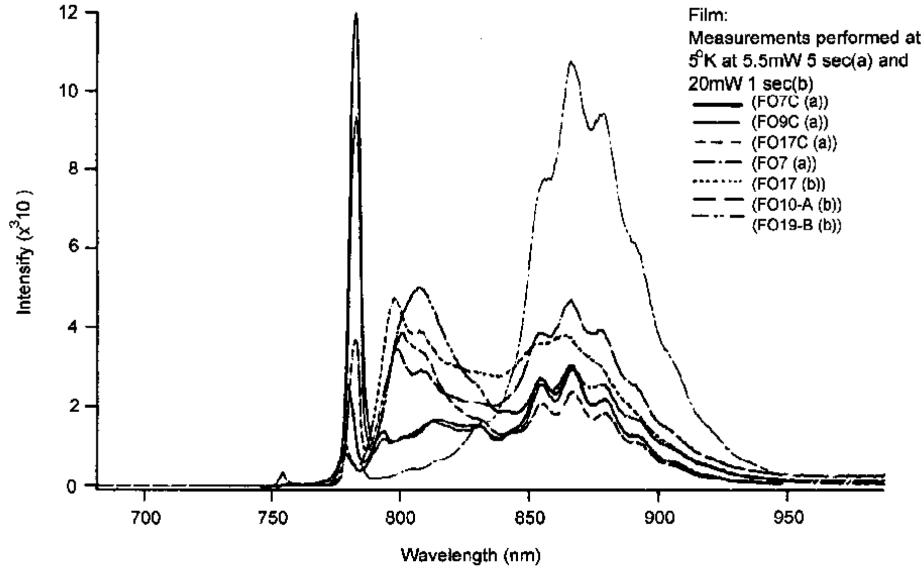


Fig. 4 PL Spectra of samples #07C, #09C, #17C, and #19C.

DLTS measurements

DLTS measurements were performed on the four $CdTe/CdS/SnO_2$/glass structures to identify the traps within the CdTe depletion region. The measurements were conducted in the temperature range from 70K to 370K. Maxima and minima in the DLTS spectrum were used to identify the type of the trap. From the Arrhenius plot of log (T/e_n) versus 1000/T, the locations of hole and electron traps were calculated. A hole was found to bc locatcd at $E_v + 0.449$ cV for samplc #07C.

Conclusion

CdS/CdTe structures were fabricated with different substrate temperatures. The effect of substrate temperature variation on the performance of CdS/CdTe structures was evaluated. It was found that open-circuit voltage values improve with increasing substrate temperature until a substrate temperature of 600°C is reached. It is believed, however, that the optimum substrate temperature is about 610°C. It is also found that high substrate temperature during CdTe evaporation passivates the film surface making the $CdCl_2$ treatment essentially ineffective. That is, the average grain size of the as deposited CdTe films increases nonlinearly with the substrate temperature following a simple series power form.

PL measurements indicate that the quality of the CdTe film improves with increasing growth temperature resulting in a decrease of pinhole density. Also, higher growth temperatures revealed the strongest near-band-edge peak indicating a relatively fewer deep traps and also the highest deep-level band (DLB) peak, indicating a low density of nonradiative recombination centers. This would imply that the number of deep level traps decreases as the film growth temperature is increased. Moreover, a reduction of the B-B (exitons) peaks with increasing CdTe film substrate temperature is also observed

DLTS measurements indicate that the number of traps is lowest for the sample with the highest substrate temperature. Just one hole trap exists at $E_v + 0.449$ eV for that sample.

Acknowledgement. The author thanks Dr. Falah Hasoon for his help in the fabrication and measurement of the CdS/CdTe structures and Pat Deppo for the PL measurements. The author also wishes to thank Dr. Larry Kazmerski and Dr. Mowafak Al-Jassim for their help and support. This work was conducted in the facilities of the National Renewable Energy Laboratory (NREL) during the author's sabbatical year.

References

[1] Ramanathan, K., Bhattacharya, R.N., Gratiata, J., Webb, J., Niles, D., Contreras, M.A., Wiesner, H., Hasoon, F.S. and Notifi, R. "Advances in the CIS Research it NREL". *Proc. of the 26th IEEE Photovoltaic Specialists Conference*, Anaheim, CA: USA, (1997), 319-322.

[2] Hermann, Allen M. "Polycrystalline Thin-film Solar Cells - A Review". *Solar Energy Materials and Solar Cells*, Univ. of Colorado, Boulder, CO, USA, 55, No. 1-2 (Sep. 1998), 75-81.

[3] Omura, K., Hanahusa, A., Arita, T., Higuchi, H., Aramoto, T., Nishio, T., Sibutani, S., Kumazawa, S., Murozono, M., Yabuuchi, Y. and Takakura, H. "Recent Technical Advances in Thin-film CdS/CdTe Solar Cells". *Renewable Energy*, 8, No. 1-4, part 1 (May-Aug. 1996), 405-409.

[4] Ferekides, C., Marinskiy, D. and Morel, D.L. "CdS: Characterization and Recent Advances in CdTe Solar Cell Performance". *Proc. of the 26th IEEE Photovoltaic Specialists Conference*, Anaheim, CA, USA, (1997), 339-342.

[5] Gordillo, G., Florez, J.M. and Hernandez, L.C. "Preparation and Characterization of CdTe Thin Films Deposited by CSS". *Solar Energy Materials and Solar Cells*, 37, No. 3-4 (July 1995), 273-281.

[6] Albin, D., Rose, D., Dhere, R., Levi, D., Woods, L., Swartzlander, A. and Sheldon, P. "Comparison Study of Close-spaced Sublimated and Chemical Bath Deposited CdS Films: Effects on CdTe Solar Cells". *Proc. of the 26th IEEE Photovoltaic Specialists Conference*, Anaheim, CA, USA, (1997), 367-370.

[7] Ferekides, C.S., Marinskiy, D., Marinskaya, S., Tetali, B., Oman, D. and Morel, D.L. "CdS Films Prepared by the Close-spaced Sublimation and Their Influence on CdTe/CdS Solar Cell Performance". *Proc. of the 25th IEEE Photovoltaic Specialists Conference*, Washington, D.C.: USA, (1996), 751-756.

[8] Khan, N.A. "Manufacture of Low-cost CdTe Solar Cells in Pakistan". *Applied Solar Energy (English translation of Geliotekhnika*, 31, No. 2 (1995), 52-58.

[9] Ramanathan, K. Dhere R. G., Coutts, T. J., Chu, T. L. and Chu, S. "CdS/CdTe Thin Film Solar Cells on Low Cost Substrates". *Proc. Of the 22th IEEE Photovoltaic Specialists Conference*, USA, (1993), 466-468.

[10] Chu, T.L., Chu, S.S., Schultz, N., Wang, C. and Wu, C.Q.". Solution-grown Cadmium Sulfide Films for Photovoltaic Devices". *J. Elecrochem. Soc.*, 139, No 9 (1992), 2443-2446.

[11] Danaher, W.J., Lyons, L.E. and Morris, G.C. "Some Properties of thin Films of Chemically Deposited Cadmium Sulphide", *Solar Energy Mat.*, 12 (1985), 137-148.

[12] Rose, D.H., Albin, D.S., Matson, R.J., Swartzlander, A.B., Li, X.S., Dhere, R.G., Asher, S., Hasoon, F.S. and Sheldon, P. "Effect of Oxygen during Close-spaced Sublimation of CdTe solar Cells". *Thin Films for Photovoltaic and Related Device Applications, Mat. Res. Soci. Symp. Proc.*, 426, San Francisco, CA: USA, (1996), 337-348.

[13] Rose, Doug H., Levi, Dean H., Matson, Rick J., Albin, David S., Dhere, Ramesh G. and Sheldon, Peter, "Role of Oxygen in CdS/CdTe Solar Cells Deposited by Close-spaced Sublimation". *Proc. of the 25th IEEE Photovoltaic Specialists Conference*, Washington, D.C.: USA, (1996), 777-780.

[14] Albin, D, Rose, D., Swartzlander, A., Moutinho, H., Hasoon, F., Asher, S.,Matson, R.. and Sheldon, P. "The Effect of Source Microstructure of the Cose-spaced Sublimation of CdTe Thin Films for Solar Cell Applications". *Mat. Res. Soc. Symp. Proc.*, 410 (1996), 45-50.

[15] Li, X., Sheldon, P., Moutinho, H. and Matson, R. "Enhanced Performance of CdS/CdTe Thin-film Devices Through Temperature Profiling Techniques Applied to Close-spaced Sublimation Deposition". *Proc. of the 25th IEEE Photovoltaic Specialists Conference*, Washington, D.C.: USA, (1996), 71-74.

[16] Chung, Gil Yong, Sonig, Jin Soo, Ahn and Byung Tae. "Effect of CdTe Stoichiometry on the Electrical Properties of CdTe Films". *Thin Films for Photovoltaic and Related Device Applications, Mat. Res. Soci. Symp. Proc.*, 426, San Francisco, CA: USA, (1996), 385-390.

[17] Dhere, R., Rose, D., Albin, D., Asher, S., Al-Jassim, M., Cheong, H., Swartzlander, A., Moutinho, H., Coutts, T., Ribelin, R. and Sheldon, P. "Influence of CdS/CdTe Interface Properties on the Device Properties". *Proc. of the 26th IEEE Photovoltaic Specialists Conference*, Anaheim, CA: USA, (1997), 435-438.

[18] Okamoto, T., Matsuzaki, Y., Amin, N., Yamada, A. and Konagai, M. "Characterization of Highly Efficient CdTe Thin Film Solar Cells by Low-temperature Photoluminescene". *Japanese Journal of Applied Physics, Part 1: Regular Papers & Short Notes & Review Papers*, 37, No. 7 (1998), 3894-3899.

خيارات لدرجة حرارة طبقة القوام لخلايا شمسية رقيقة الغشاء، متعددة التبلور، مصنوعة من كاديوم تيلورايد النامي بطريقة التسامي عن قرب

عبد الرحمن محمد العمود

قسم الهندسة الكهربائية ، كلية الهندسة،جامعة الملك سعود ، ص .ب ٨٠٠ ،

الرياض ١١٤٢١ ، المملكة العربية السعودية

(قدم للنشر في ٢٥/٠٧/٢٠٠٠م، وقبل للنشر في ٢٣/٠٥/٢٠٠١م)

ملخص البحث. يقدم هذا البحث دراسة مميزة ، لأغشية رقيقة من الكاديوم تيلورايد (CdTe) نامية بطريقة التسامي عن قرب (CSS)، بواسطة عدة طرق : المطيافية العابرة العميقة (DLTS)، الإجهارية الإلكترونية الماسحة (SEM)، والتلألؤ الضوئي (PL). وتم ملاحظة تأثير درجة حرارة طبقة القوام (substrate) على أداء النبيطة ، وخصائص مواجهة الطبقات (interface) وخصائص جسم المادة (bulk) .