J. King Saud Univ., Vol. **3**, *Eng. Sci.* (1), pp. 19–43 (1411H/1991)

Time-Ratio Control of Chopper-Type AC Voltage Regulators

K.E. Ad'doweesh, A.L. Mohamadein and H.A. Al-Ghalaban
Electrical Engineering Department, College of Engineering, King Saud University, P.O. Box 800, Riyadh 11421, Saudi Arabia

Abstract. This paper discusses an improved technique and a completed design of a microprocessor-based AC voltage regulator circuit. The proposed regulator is working in the chopping mode and hence presents improvements in its performance characterized by:

a) Control range is independent of load phase angle.
b) Linear relationship is almost achieved between time ratio and amplitude of fundamental component of load voltage.
c) Order of dominant load voltage harmonics can be controlled through changing chopping frequency.

The designed controller employs Z80 microprocessor. Flow chart of the program used along with system hardware are provided. Experimental and related theoretical results for controller performance on static loads are presented. Moreover, a comparison with the phase-angle control strategy is presented demonstrating the merits inherited by the proposed scheme.

1. Introduction

The utilization of solid state switching devices in electrical power control contributed to the evolution of wide varieties of applications. This is mainly attributed to the advantages possessed by these devices as fast response, compactness, low losses and low power needed in its control circuitry. The systems developed so far can be classified into two main categories being either of the supply conditioning or load conditioning versions. Supply conditining can be achieved using controlled converters, choppers for DC applications and inverters, cycloconverters and AC voltage regulators for AC applications. Load conditioning is achieved by incorporating switching devices in the load circuit such as power factor correction using switched capacitors and similar applications. AC voltage regulator, as one of the supply conditioning systems, is employed whenever a variable AC supply is required. This is achieved by connecting a series switch between fixed AC supply and the load, where-

upon, power flow can be controlled by controlling conduction periods of the switch. The most common applications of AC voltage regulators are: industrial heating, on-load transformer tap changing, light control, speed control of induction motors and AC magnet controls. Conventionally, AC voltage regulators employ phase angle control technique [1]. Such a technique, though being simple and less expensive from circuitry point of view but suffers from disadvantages as:

a) Range of delay angle is controlled by load phase angle.

b) Input power factor depends on the delay angle and is in general low especially at low output voltage ranges.

c) The dominant harmonic order of the output voltage is the third and harmonic contents are high.

In fact, the order of the dominant harmonic could be increased by chopping the input voltage at a high frequency, thus leading to the improvement of the input power factor and reduction of the harmonic contents. These forced-commutation techniques are becoming attractive with the advancement of power semiconductor devices (*e.g.* gate-turn-off thyristors) [2].

The order of the dominant harmonic is increased to a value equals the number of pulses and gaps in a half-cycle [3]. The ability and flexibility of the microprocessor simplified the problem of control circuit. The following sections discuss the design of a microprocessor based AC voltage regulator utilizing the above mentioned technique in more details.

Power Circuit

The circuit is mainly composed of two switches; series switch and parallel one (Fig. 1). Each switch is a pair of GTOs connected in inverse-parallel. The series switch is used to chop the input supply while the other one is used only with inductive loads as a flywheel to give a path to the current passing in the load. The circuit can be simplified by replacing the two invers-parallel GTOs with only one GTO with diodes bridge as shown in Fig. 2. This configuration of the circuit has advantages of using only one GTO as a switch beside the simplicity of the firing circuit.

The selection of the Gate drive circuit is very important in GTO characteristics [4,5]. The self turn-off capability, high di/dt rating of the GTO, fast switching speed and high power rating are affected by the gate drive and snubber design which are the most critical steps in the application of high-power GTO's.

Hardware Overview [6]

Fig. 3 illustrates the block diagram of the implementation of the controller hardware circuit. The Z80-CTC timer chip contains four channels which can operate

in a number of different modes as determined by the program. The EPROM is used to store the program while the desired look-up table is stored in the RAM. The values of the duty cycle (K) and the number of pulse per half cycle (N) are read via the PIO. The additional hardware required to complete the control circuit are: latching flip-flop, drive circuits, optical isolators to electrically isolate the microprocessor system from the A.C. chopper circuit and a zero crossing detector. The design of this last item is important since it provides the timing reference for the system.

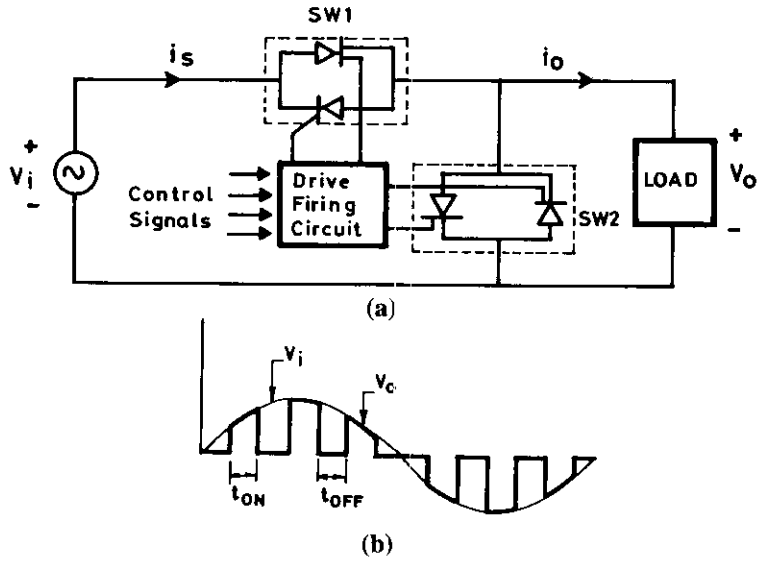


Fig. 1. Chopper mode AC voltage controller
a) circuit b) output voltage (N = 3)

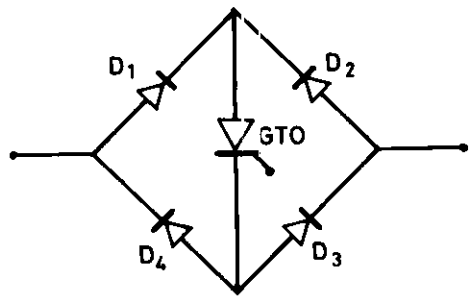


Fig. 2. Single GTO switch

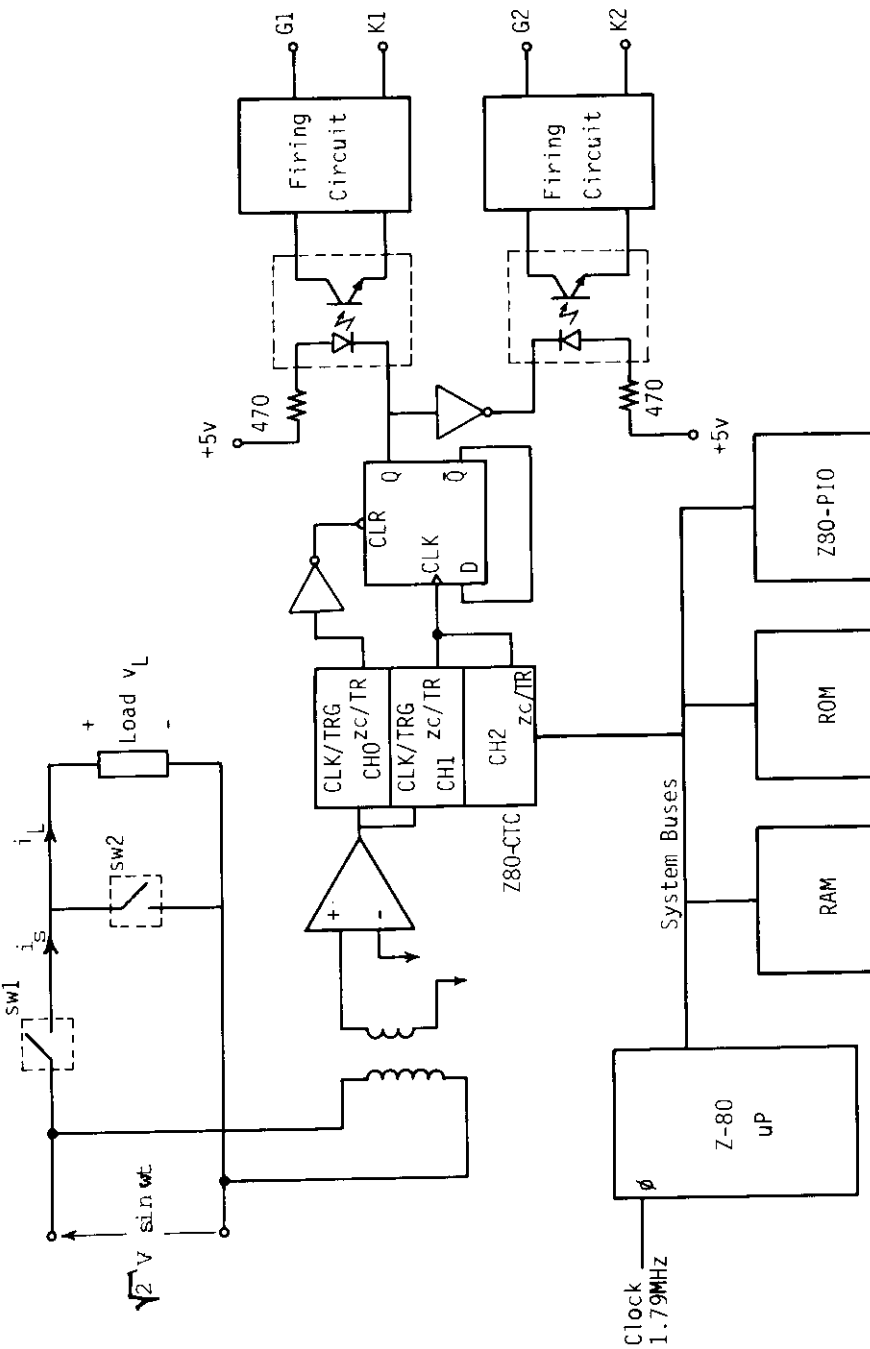


Fig. 3. AC voltage controller and the interface with the microprocessor

Programming the Z80 to Generate the Control Signals

Measuring the Frequency

The Z80 microprocessor at the first time measures the frequency of the supply. This is done by programming ch0 of Z80-CTC as a counter with the interrupt enabled and ch1 as a timer with external rising edge triggering. The time constants loaded to the timer and the counter are FF_H and 2 respectively. The first rising edge of the zero-crossing detector output initiates the timer downcounting while the second rising edge (end of cycle) causes ch0 counter to interrupt the microprocessor. The interrupt service routine (ISR1) serving ch0 reads the timer and computes the supply frequency, as shown in Fig. 4.

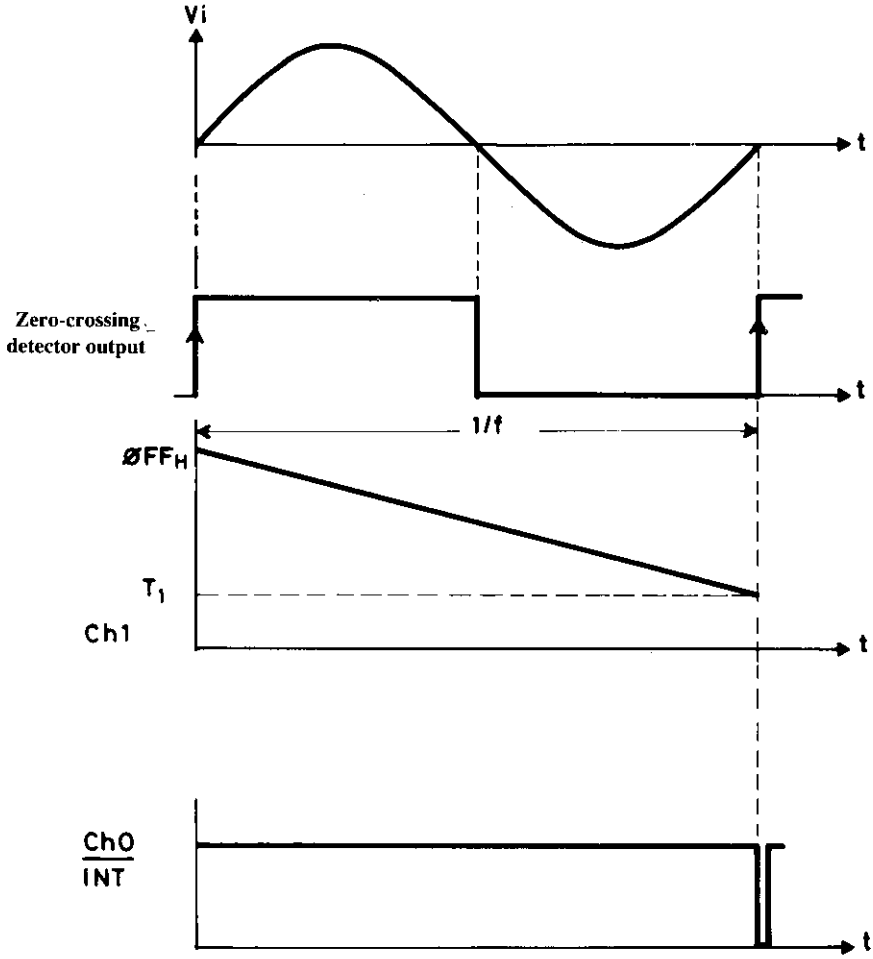


Fig. 4. Measuring the supply frequency

Producing the Pattern of Gate Signals

According to the required duty cycle [$K = t_{ON}/(t_{ON} + t_{OFF})$] and the number of pulses per half cycle (N), the microprocessor uses the value of the already measured frequency to compute the widths of "ON" and "OFF pulses utilizing equations (3, 4 or 8, 9), given later.

Pulses and gaps widths of quarter of the cycle are computed according to the upper-mentioned equations and saved in a look-up table whose starting address is kept in a pointer. Because of quarter and half symmetry only first quarter gaps and pulses are needed. The rest of table containing all values and gaps for the complete cycle is generated using the first computed values by sorting them according to the specified symmetries. This saves a lot of microprocessor time. Although, the generated waveform in this case is the time ratio control with quarter-wave symmetry, the program is designed in a way to generate any pulse pattern of the values contained in the look-up table. Hence, it is possible to generate some other waveforms like PWM waveforms.

Ch0 and ch2 of the Z80-CTC are then programmed to operate as counters with enabled interrupts served by the interrupt service routines: ISR2, ISR3 respectively. Ch0 is triggered by the rising edge of the zero-crossing detector and requests an interrupt at the beginning of every cycle. ISR2 is used to initialize the pointer to the top of the table and to program ch1 as a timer with automatic triggering. ISR2 also sends the first value at the top of the look-up table to ch1 folowed by the next. Ch1 output is used as a clock of ch2. Ch2 which contains a value equals 1 when triggered by the output of ch1, requests an interrupt. In the cases where the width of a pulse or gap is too long to be represented by an 8-bit word, ch2 can be used ot form a 16-bit down-counter with ch1. In this case, the output should be taken from ch2. While ch1 is down-counting it is supplied with the next pulse or gap width from the look-up table by the ISR3. The required signal pattern is generated on a flip-flop output. The flip-flop is cleared with the beginning of each supply cycle thus giving a waveform beginning with a gap. the time-out signal of ch1 toggles the state of the output of the flip-flop. The firing logic for the fly-wheeling switch is the complement of the series switch. Hence the output of flip-flop is inverted to feed the firing circuit of the fly-wheeling switch. Fig. 5 shows the flowcharts of the main program and the ISRs.

Synchronization

In practical system the delay times can never be generated exactly. There is thus, a tendency for the interrupt train to drift. Synchronization of the firing logic with supply voltage is kept as the pointer to look-up table is initialized to its starting address with the beginning of each supply cycle.

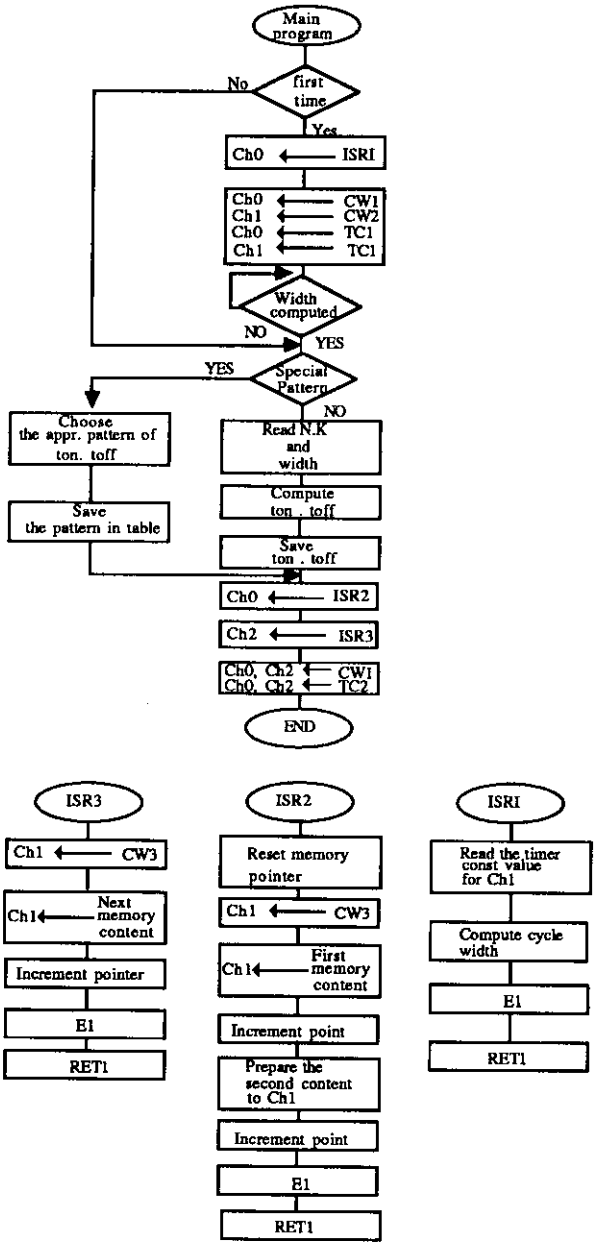


Fig. 5. Flowcharts of the main program and ISRs

Analysis

Analytical evaluation of chopper performance can be achieved by determining harmonic contents in output load voltage. In the analysis switching transients in load voltage have been ignored and hence, its wave form will be as that shown in Fig. 6-a for the case of 3 pulses and four gaps per half cycle. Moreover, firing instants of the GTO's are selected such that the wave is always symmetrical around $\pi/2$. Such a technique was used to avoid the presence of phase shift-between the fundamental components of load and supply voltages.

Fourier analysis for the wave shown in Fig. 6-a in its general form with N pulses per half cycle will yield sine terms of odd orders only whose rms values are given by

$$V_n = \frac{2}{\pi\sqrt{2}} \int_{\alpha_1, \alpha_3, \alpha_5, \ldots, \alpha_{(2N-1)}}^{\alpha_2, \alpha_4, \alpha_6, \ldots, \alpha_{2N}} V_m \sin \omega t \sin n\omega t \, d\omega t \qquad n = 1,3,5,7,\ldots (1)$$

where α's are the values of switching angles, which are determined according to the value of the time ratio 'K' as follows:

$$K \text{ (time ratio)} = t_{ON} / (t_{ON} + t_{OFF}) \leq 1.0 \qquad (2)$$

For a wave having N pulses and (N+1) gaps per half cycle *i.e.* wave starting with zero, then; pulse and gap angular durations are given by;

$$\alpha_{ON} = \pi \frac{K}{N + 1 - K} \qquad (3)$$

and

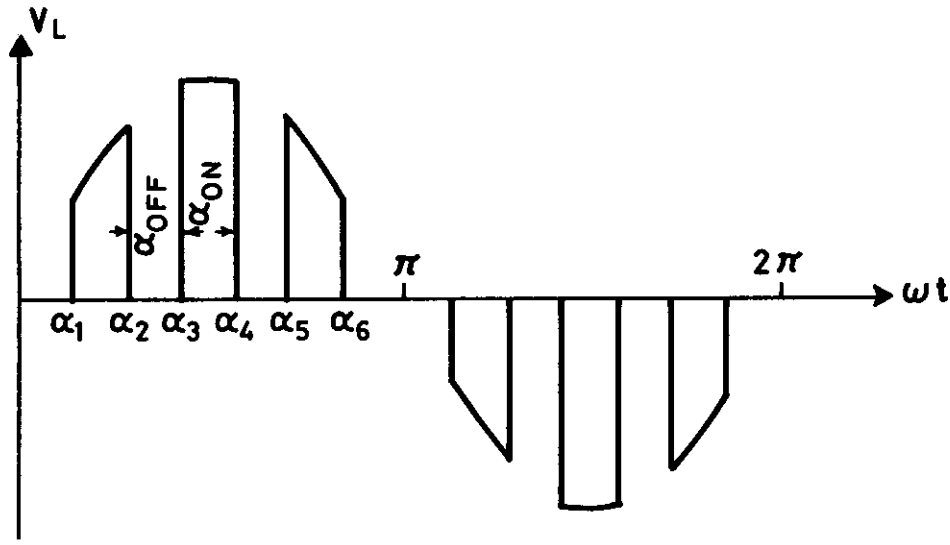
$$\alpha_{OFF} = \pi \frac{(1 - K)}{N + 1 - K} \qquad (4)$$

Therefore;

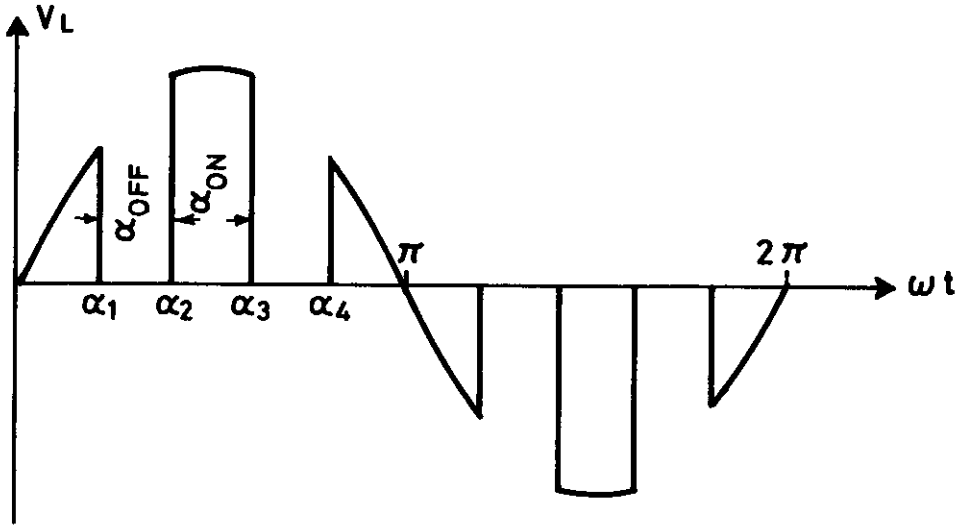
$$\alpha_J = [\, J-(J \text{ MOD } 2)]/2 \,.\, [(\alpha_{ON} + \alpha_{OFF}) + (J \text{ MOD } 2)] \,.\, \alpha_{OFF}$$

$$J = 1,2,3, \ldots (5)$$

On the other hand, with time ratio control, there exist another possible firing control strategy in which case the output voltage waveform starts with a pulse. Therefore, output voltage waveshape will be made up from N pulses and (N–1) gaps per half cycle, see Fig. 6-b. Symmetry of output voltage waveform around $\pi/2$ is being



(a)



(b)

Fig. 6. Load voltage waveform for time ratio control

also kept in this case to ensure zero phase shift between fundamental component of load and supply voltages. Under these conditions, rms values of the harmonics in load voltage will be given by:

$$V_n = \frac{2}{\pi\sqrt{2}} \int_{0,\,\alpha_2,\,\alpha_4,\,\ldots,\,\alpha_{(2N-2)}}^{\alpha_1,\,\alpha_3,\,\ldots,\,\alpha_{2N-3},\,\pi} V_m \sin\omega t \sin n\omega t \, d\omega t \qquad n = 1,3,5,\ldots(6)$$

where α's are given by

$$\alpha_J = [\,J-(J \text{ MOD } 2)]/2 \,.\, [(\alpha_{ON} + \alpha_{OFF}) + (J \text{ MOD } 2)] \,.\, \alpha_{ON}$$

$$J = 1,2,3, \ldots (7)$$

α_{ON} and α_{OFF} are given by;

$$\alpha_{ON} = \pi \frac{K}{N + K - 1} \tag{8}$$

and

$$\alpha_{OFF} = \pi \frac{(1 - K)}{N + K - 1} \tag{9}$$

where; the time ratio "K" is given by equation (2).

Having evaluated harmonic contents in load voltage, load current can be eventually determined. For a static inductive load of resistance R and inductance L, then rms values of the harmonic components of load current are given by:

$$I_n = \frac{V_n}{\sqrt{R^2 + n^2\omega^2 L^2}} \Big\lfloor -\tan^{-1}\frac{n\omega L}{R}$$

Consequently, effective values of load current and voltage can be calculated as follows

$$I_L = \Big[\sum_{m=1}^{\infty} I_m^2 \Big]^{1/2}$$

$$V_L = \Big[\sum_{m=1}^{\infty} V_m^2 \Big]^{1/2} \tag{11}$$

It follows then that load power factor will be equal to

$$PF_L = \frac{I_L}{V_L} . R = \frac{I_L Z_1}{V_L} . \cos \phi_1 \tag{12}$$

Where; $Z_1 = \sqrt{R^2 + (\omega L)^2}$

$$\phi_1 = \text{displacement angle} = \tan^{-1} \frac{\omega L}{R}$$

As far as supply side is concerned, time variation of input supply current is determined as follows:

$$i_s(t) \begin{cases} = \sum_{m=1}^{\infty} \sqrt{2}\, I_m \sin(m\omega t - \phi_m); & \text{sw1 on} \\ = 0 & \text{; sw2 off} \end{cases} \tag{13}$$

where; $\phi_m = \tan^{-1} \frac{m\omega L}{R}$

Consequently, effective value of supply current is determined by;

$$I_{s_{rms}} = \left[\frac{1}{2\pi} \int_0^{2\pi} i_s^2(t)\, d\omega t \right]^{\frac{1}{2}}$$

or

$$I_{s_{rms}} = \left[\sum_{m=1}^{\infty} I_{s_m} \right]^{\frac{1}{2}} \tag{14}$$

where; I_{s_m} is the rms value of the m^{th} component of supply current. Moreover, the rms value and the phase of the fundamental component of input supply current can be obtained as follows:

$$A_1 = 2f \int_0^{1/f} i_s(t) . \sin \omega t\, dt \tag{15}$$

and

$$B_1 = 2f \int_0^{1/f} i_s(t).\cos \omega t \, dt \tag{16}$$

where, f is the frequency of the supply voltage.
Hence,

$$I_{s_1} = \sqrt{\frac{A_1^2 + B_1^2}{2}} \tag{17}$$

and

$$\phi_{s_1} = \tan^{-1}(B_1/A_1) \tag{18}$$

Therefore, chopper power factor as measured from supply side is given by:

$$PF_s = \frac{I_{s1} \cdot \cos \phi_{s1}}{I_s} \tag{19}$$

Harmonic factor in input supply current "HF_S" is given by:

$$HF_s = \sqrt{\left(\frac{I_s}{I_{s1}}\right)^2 - 1} \tag{20}$$

Results

The regulator circuit outlined earlier has been tested when feeding static inductive loads of phase angles of 30° and 60° respectively. Number of pulses per half cycle were set to be equal to 5,7 and 9 respectively. Load and supply effective values of currents as well as effective value of load voltage were recorded for various values of time ratio "K". Moreover, an HP-3580A spectrum analyser was employed to determine harmonic contents in supply current as well as load voltage and current. The validity of computation have been ascertained by comparing load and supply currents wave forms with test results, see Fig. 7.

Variation of Load Voltage and Current Harmonic Content Versus Time Ratio "K"

One of the main characteristics to be determined is the way in which harmonic content varies as the value of "K" is changed. Theoretical results related to harmonic variations versus "K" for cases of 5, 7 and 9 pulses per half cycle for a load voltage starting with a gap are shown in Fig. 8. Moreover, experimental values show good

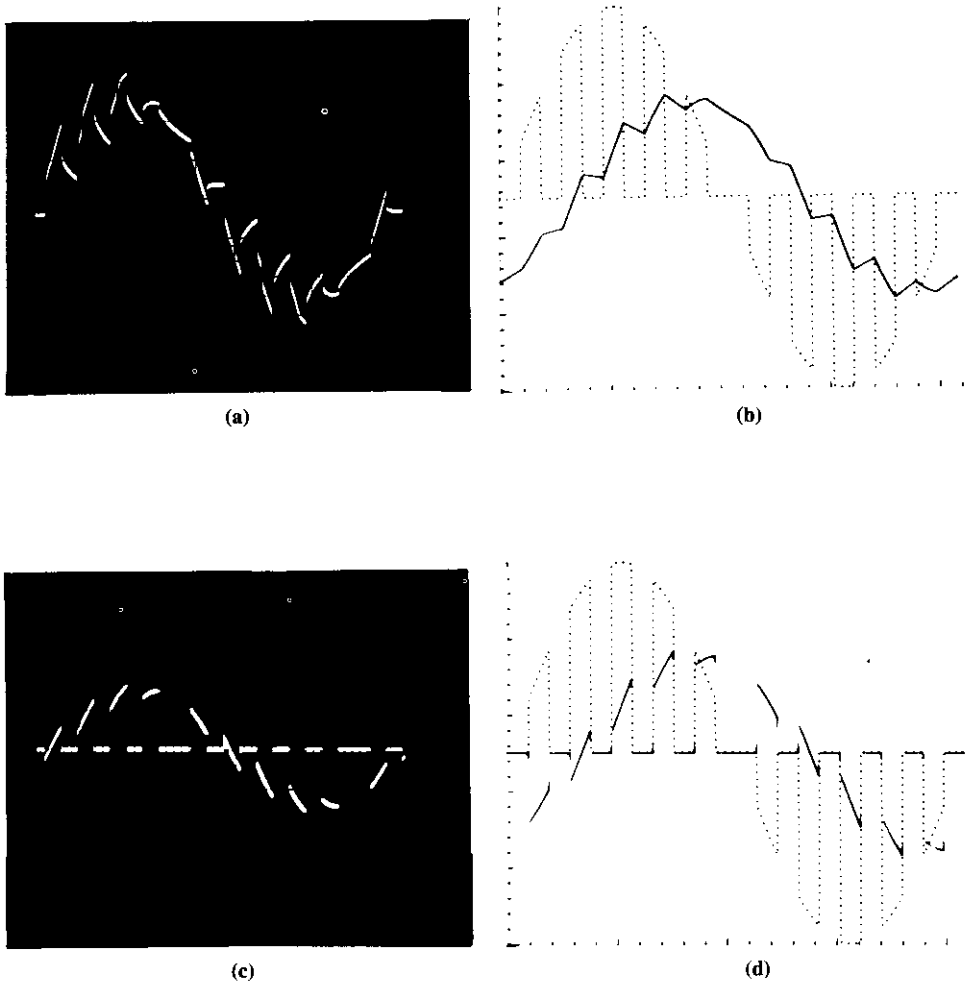


Fig. 7. Load and supply currents, for N = 5, K = 0.5, and $\Phi = 60°$
a) measured load current, b) simulated load current
c) measured supply current, d) simulated supply current

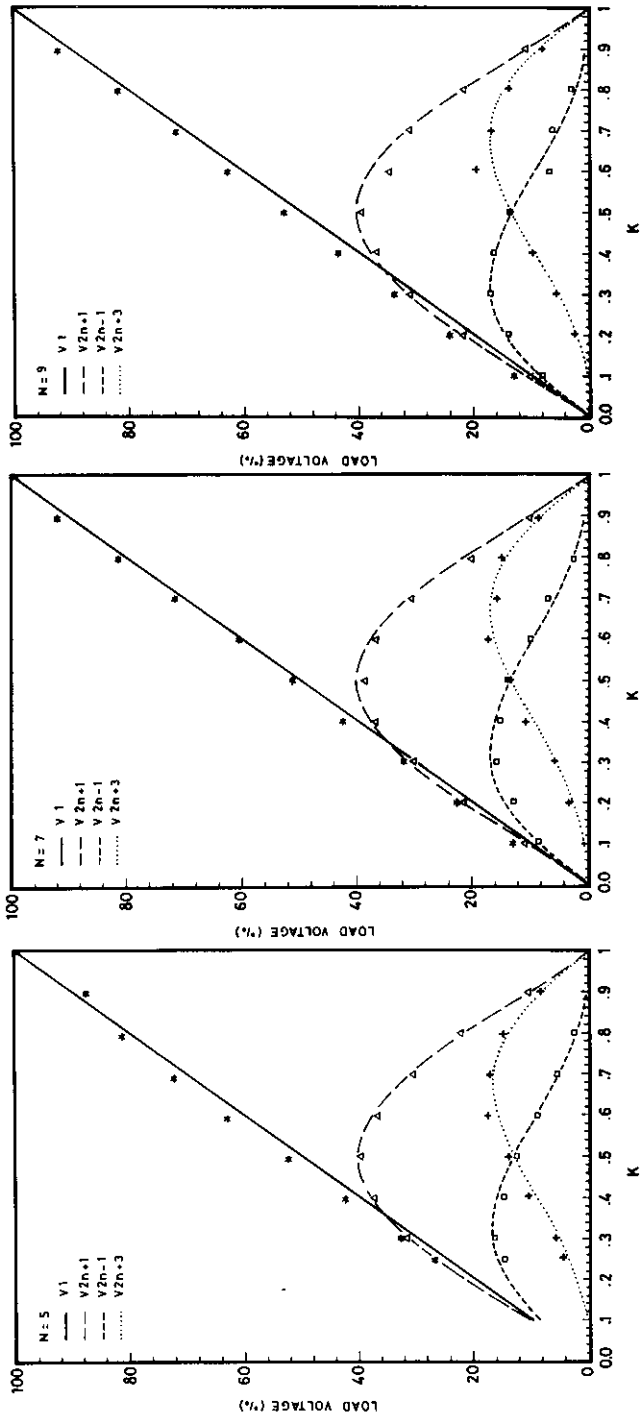


Fig. 8. Variation of load voltage harmonic contents versus "K" for N = 5,7 & 9. Test points and computed results

correlation with relevant predicted values. A salient feature with this type of controllers is the almost linear relationship existing between the amplitude of the fundamental component in load voltage and the time ratio "K", for control stategies using more than 5 pulses per half cycle. Therefore, with a fair degree of accuracy, it could be stated that,

$$V_{LI} = K \cdot V_m \tag{21}$$

A proof for the above mentioned relationship is given in appendix (1). Regarding harmonic content, the dominant harmonic in output load voltage has the order of $(2N \pm 1)$. The "+" sign applies for a load voltage wave form starting with gap while the "–" sign is for a pulse started wave shape. Moreover, the dominant harmonic is side-banded by other two harmonics of the order $[(2N+1) \pm 2]$.

With reference to Fig. 8 it could be observed that the peak values of dominant and side band harmonics are constant irrespective of the value of number of pulses per half cycle ($N \geq 1$). The peak value of the dominant harmonic reaches 40% at $K = 0.5$ while side band harmonics showed a peak of 18% at $K \simeq 0.3$ and 0.7 for the upper and lower order harmonics respectively. Such a finding could be well made use of in suppressing these harmonics through increasing "N" and adding a reasonable value of inductance in series with the load. Such a finding is clearly demonstrated by Fig. 9 which shows harmonic currents variations versus "K" for N = 5, 7 and 9 respectively with an inductive load of phase angle 30°.

Variation of R.M.S. Values of Currents and Voltage Versus "K"

The way in which the r.m.s. values of load and supply currents vary with time ratio factor "K" for N = 5, 7 and 9, and load phase angle of 60° lagging are shown in Fig. 10 respectively. Load phase angle was chosen to be highly lagging to demonstrate the effect of the free wheeling circuit. In general, the r.m.s. value of load current varies almost linearly with "K". This implies that the r.m.s. of harmonic content in load current represents a quite low proportion. Moreover, presence of free wheeling circuit resulted in a decrease in the value of r.m.s. value of supply current compared to load current. Consequently, an improvement in the power factor as seen from the supply side is to be expected. On the other hand, it could be noticed that changing number of pulses per half cycle from 5 to 9 has resulted in slight changes in rms values of load and supply currents at the same value of K. Same findings apply also to rms value of load voltage.

Controller Supply and Load Power Factors

One of the main drawbacks of solid state AC voltage controllers is their inherent low values of power factor at low output voltage levels even with a purely resistive load. However, with the proposed chopper type AC voltage controller, power factor

is expected to be higher than conventional phase angle control type. This is an outcome of the suppressive effect offered by load inductance added to free wheeling action. The variations of load and supply power factors versus "K" for N = 5, 7 and 9 and with load phase angle of 60g are shown in Fig. 11. The effect of increasing "N" on power factors appears significatnly at low values of "K" when load voltage harmonics represnet an appreciable proportion. For example at K = 0.1, load power factor is 0.23 at N = 9, 0.2 for N = 7 and 0.18 at N = 5. The values of the power factor as seen from the supply side are slightly higher than corresponding values as seen from load side.

On the other hand, the values of power factor under same loading conditions with phase angel control are shown inFig. 11. It is evident that the proposed chopper type AC voltage regulator offers higher values of power factor as measured from either load or supply sides.

Variation of Current Harmonic Factors Versus Fundamental Load Voltage Component

Harmonic factors at both supply and load sides were evaluated with different values of number of pulses per half cycle as well as various load phase angles.

Variation of harmonic factor for supply current with changes in fundamental component of load voltage at N = '5, 7 and 9 and phase of 30° are shown in Fig. 12. Moreover, on the same figure relevant values are shown for phase angle control (PAC) technique. it is clear that increasing number of pulses per half cycle leads to a decrease in the harmonic factor of supply current. On the other hand, phase angle control strategy has lower values of harmonic factors.

The effect of load phase angle on supply current harmonic factor can be visualized by referring to Figs. 12 and 13 which show variations in the latter with N = 9 and load phase angles of 30° and 60°. It is clear that with highly inductive loads, supply current HF increases especially at low values of output load voltage.

On the other hand, variations in load current harmonic factor with changes in load voltage fundamental component are shown in Fig. 14 for N = 9 and load phase angles of 30° and 60°. It is evident that;

(a) Increasing load phase angle (*i.e.* increasing its inductive part), produces more suppressive effect on harmonis in load current.

(b) Presence of free wheeling circuit contributes to continuous flow of load current maintaining that load circuit contains a reasonable amount of inductance.

Therefore, load current HF in general has low values compared to supply current HF for $\phi_L \geq 0$. For loads with zero inductive part load and supply currents HF's become equal. On the other hand, increase in load phase angle produces consequent decrease in load current HF as can be seen from Fig. 14.

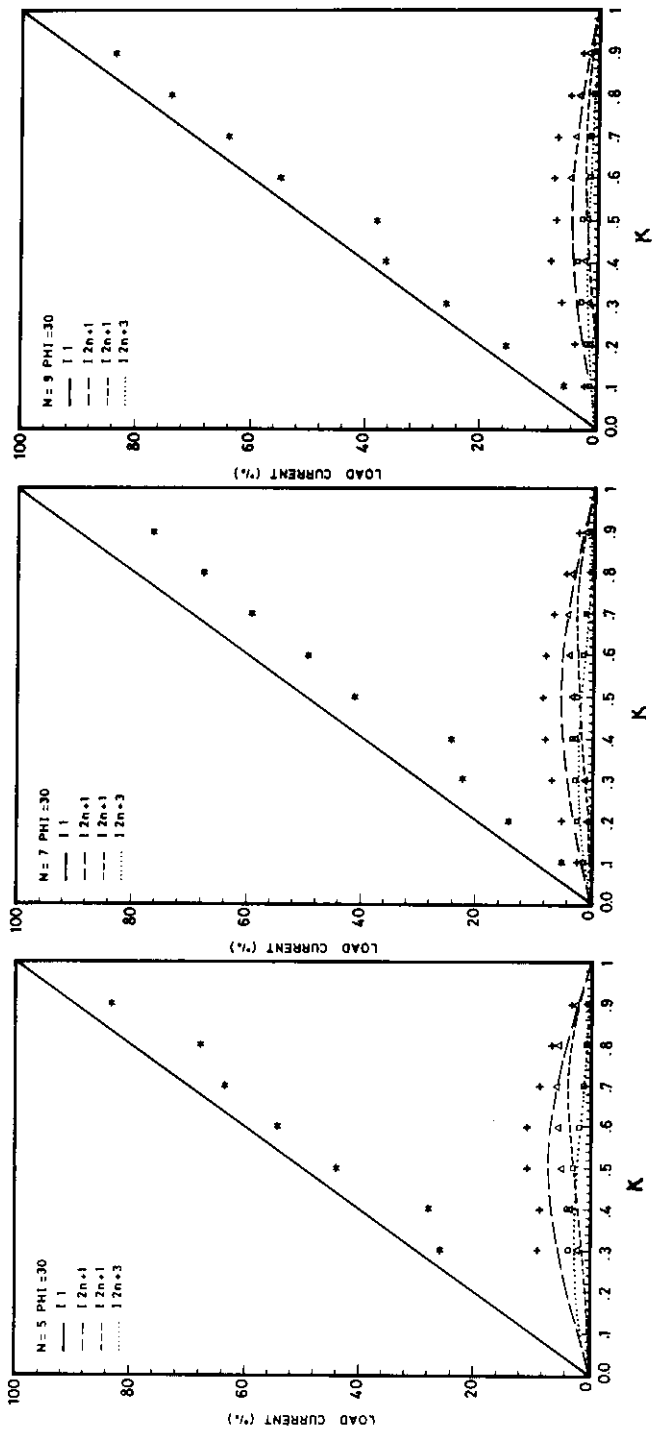


Fig. 9. Variation of load current harmonic contents versus "K" for N = 5,7 & 9. Test points and computed results

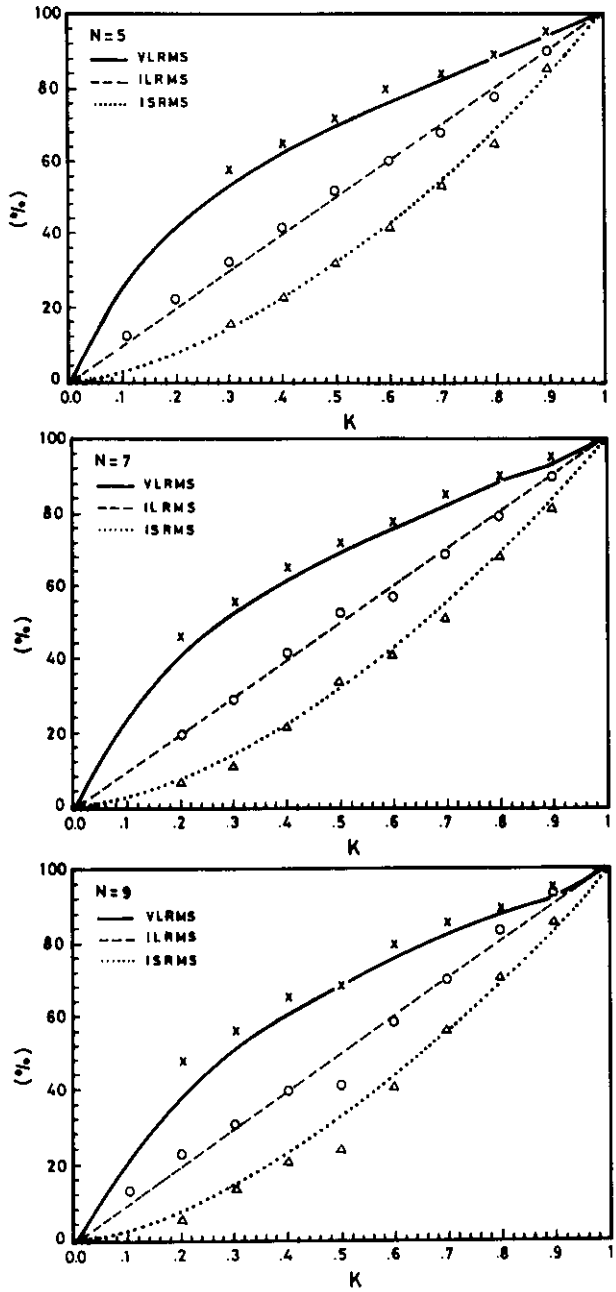


Fig. 10. Variation of R.M.S. values of load voltage, load current and supply current versus "K" for N = 5, 7 & 9. Test points and computed results

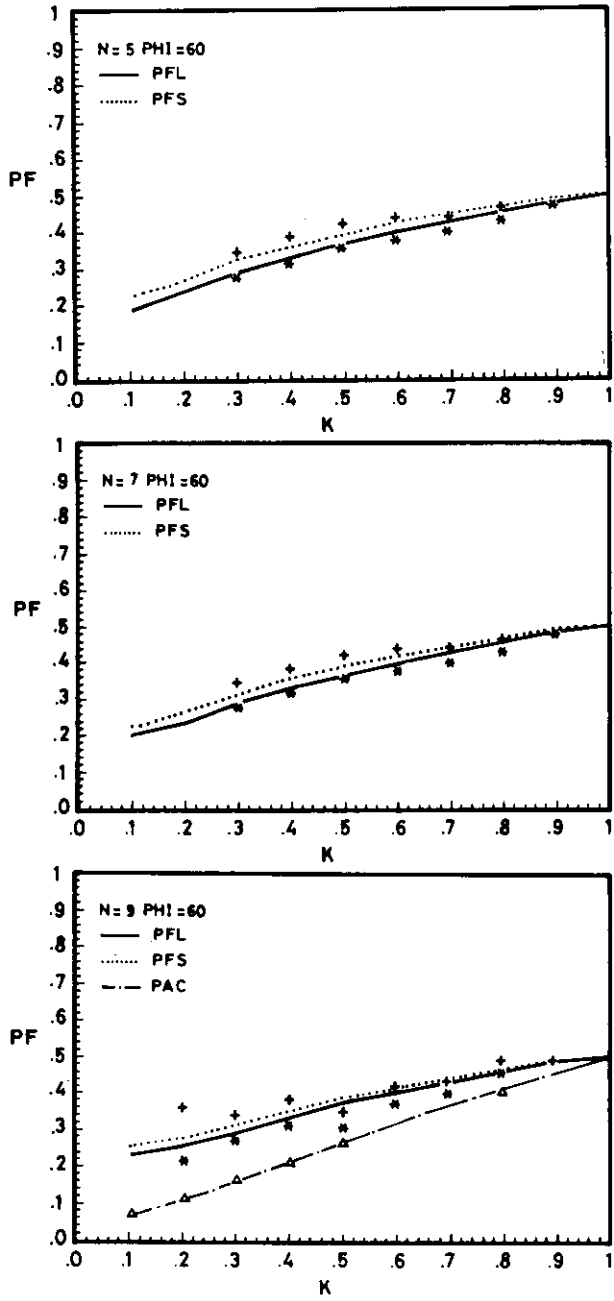


Fig. 11. Variation of load and supply power factor versus "K" for N = 5, 7 & 9, $\Phi = 60°$ (inductive). Test points and computed curves

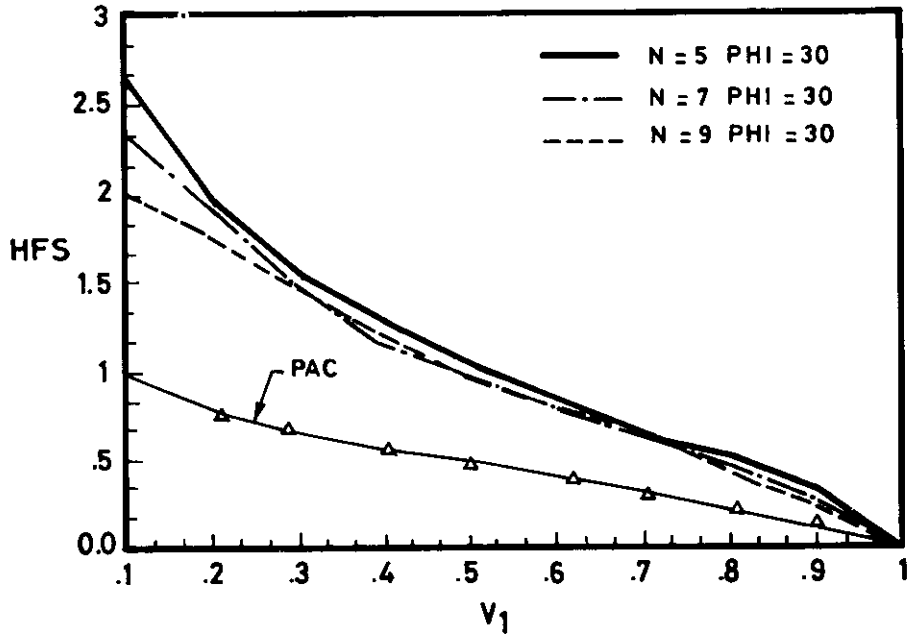


Fig. 12. Variation of supply current harmonic factor versus V_1 for $\Phi = 30°$ inductive

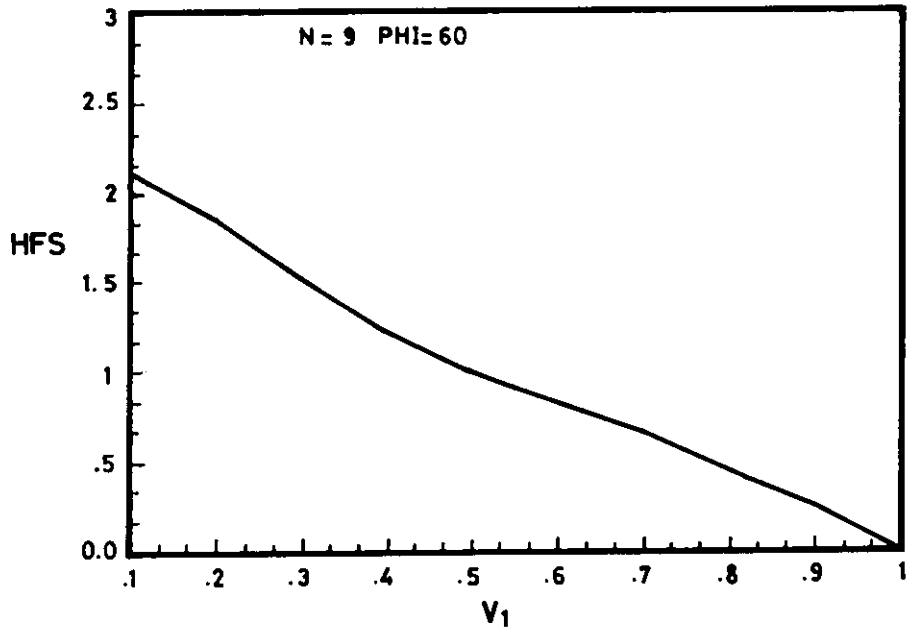
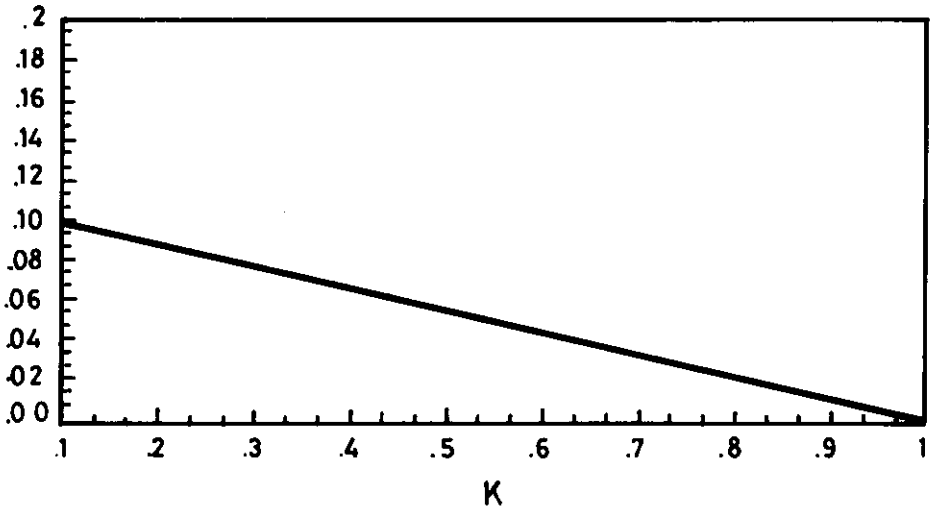
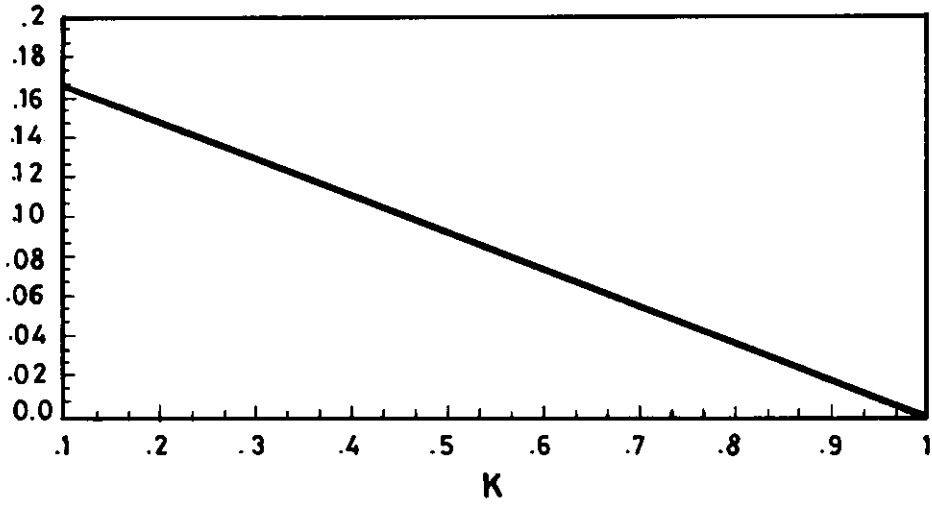


Fig. 13. Variation of supply current harmonic factor versus V_1 for N = 9 & $\Phi = 60°$ (inductive)



(a)



(b)

Fig. 14. Variation of load current harmonic factor versus V_1 for N = 9 a) $\Phi = 60°$ b) $\Phi = 30°$ inductive

Conclusions

This paper presents a Z-80 microprocessor system which is designed to perform the following functions: (a) measuring the line frequency, (b) calculating the pulses widths, (c) ensuring synchronization with supply voltage and (d) generating the pulse patterns to control the AC chopper circuit.

Experimental and corresponding theoretical results of operating this voltage regulator circuit in the time-ratio mode are presented showing improved overall performance when compared to conventional PAC type. It has been shown, that the relation between the amplitude of the fundamental component of both the load current and voltage and the time ratio K is almost linear especially for higher values of N. Moreover, the order of the dominant harmonics depends on the value of N, thereby giving a possibility for suppressing them in the load current with a reasonable load inductance at high values of B. Also, as compared to the conventional PAC technique, the power factor is improved. On the other hand, controllabilit of load voltage in PAC technique, implies load current discontinuity while voltage control in the proposed regulator is achieved with continuous load current flow due to freewheeling action. Such a finding is of a prime importance when dynamic loads are used.

Acknowledgement. The authors are grateful to the Research Center, College of Engineering, King Saud University, Riyadh, Saudi Arabia, for research facilities provided. Thanks are also extended to Mr. M. Tibawi, a research assistant for the help provided.

References

[1] Shephard, W. *Thyristor Control of AC Circuit.* London: William Clowes & Sons Limited, 1976.

[2] Ad'doweesh, K. "Microprocessor Based AC Voltage Control Using GTO Thyristors." *Proc. of ISMM International Symposium Mini and Micro and their Applications,* Lugano, Switzerland, (June, 1987), pp. 83–86.

[3] Mohamadein, A. and Ad'doweesh, K. "Evaluation of the Performance of the Chopper Type AC Voltage Controllers." *Intern. Journ. of Electronics,* 67, No. 4 (1989), 666–683, U.K.

[4] Ho, E. and Sen, P. "Effects of Gate-drive circuit on GTO Thyristor Characteristics." *IEEE Transactions on Industrial Electronics,* Vol. IE, 33, No. 3 (1986), pp. 325–331.

[5] Biswas, S. "An Autoprotecting Gate Drive Circuit for GTO Thyristors." *"IEEE Transactions on Industry Application,* Vol. IA, 24, No. 1 (1988), pp. 121–126.

[6] Ad'doweesh, K.E.; Mohamadein, A.L. and Ghalban, H., "Microprocessor Based Controller for AC Chopper." *Proc. of the 11th National Computer Conference,* Dhahran, (4–7 Mar 1989), pp. 483–493.

Appendix (1)

The fundamental component of the load voltage shown in Fig. 6-a is given by;

$$V_1 = \frac{2}{\pi} \int_{\alpha_1,\alpha_3,\ldots,\alpha_{2N-1}}^{\alpha_2,\alpha_4,\ldots,\alpha_{2N}} V_m \sin^2 \omega t \, d\omega t$$

where; N = Number of pulses per half cycle.
The previous equation yields;

$$V_1 = \frac{V_m}{\pi} \left[(\alpha_2 - \alpha_1) + (\alpha_4 - \alpha_3) \ldots + (\alpha_{2N} - \alpha_{2N-1}) \right]$$

$$- \frac{V_m}{2\pi} \left[\sin 2\alpha_2 - \sin 2\alpha_1 + \sin 2\alpha_4 - \sin 2\alpha_3 \ldots . \right.$$

$$\left. + \sin 2\alpha_{2N} - \sin 2\alpha_{2N-1} \right]$$

$$= \frac{V_m}{\pi} . N.\alpha_{ON} - \frac{V_m}{2\pi} \left[\sin 2\alpha_2 + \sin 2\alpha_4 + \ldots \sin 2\alpha_{2N} \right]$$

$$+ \frac{V_m}{2\pi} \left[\sin 2\alpha_1 + \sin 2\alpha_3 + \ldots \sin 2\alpha_{2N-1} \right]$$

The terms $2\alpha_2, 2\alpha_4, \ldots, 2\alpha_{2N}$ are is ascending order with an increment of α_x. Same applies for $2\alpha_1, 2\alpha_3, \ldots, 2\alpha_{2N-1}$. It could be proved that;

$$\sin\theta + (\theta+\psi) + \sin(\theta+2\psi) + \ldots + \sin[\theta+(N-1)\psi] = \frac{\sin\frac{N\psi}{2}}{\sin\frac{\psi}{2}} \cdot \sin[\theta + (\frac{N-1}{2})\psi]$$

Consequently, V_1 is then given by;

$$V_1 = V_m \cdot \frac{N}{N+1-K} K + \frac{V_m}{\pi} \cdot \frac{\sin\alpha_{ON} \cdot \sin\alpha_{OFF}}{\sin(\alpha_{ON} + \alpha_{OFF})}$$

$$= g_1 + b_1$$

The terms g_1 and b_1 when evaluated for different values of K are shown in Fig. 15 for N = 1, 3 and 9 respectively. It is clear that g_1 dominates the value of V_1 while b_1 becomes less effective as N-increases and even reaches negligible order as $N \geqslant 3$. Therefore, for large values of "N";

$$V_1 \simeq V_m \frac{N}{N+1-K} \cdot K \simeq V_m \cdot K$$

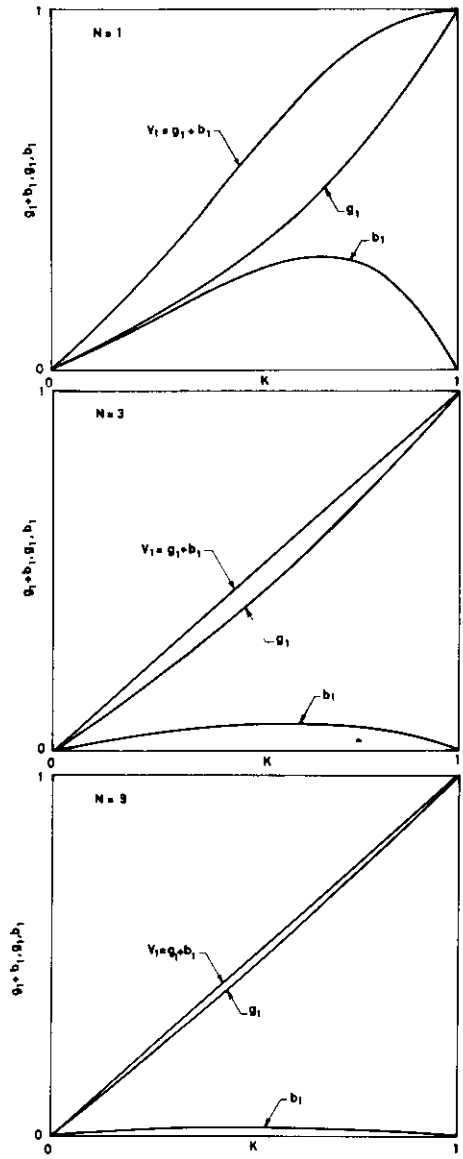


Fig. 1. Relation between g and b_1 evaluated for different values of K

التحكم بنسبة الوقت لمنظم الجهد المتردد من نوع المقطع

خالد إبراهيم الدويش، عادل لطفي محمدين وحيدر أحمد الغلبان

قسم الهندسة الكهربائية، كلية الهندسة، جامعة الملك سعود، ص.ب ٨٠٠، الرياض ١١٤٢١، المملكة العربية السعودية

ملخص البحث. يدرس هذا البحث طريقة محسنة مع التصميم الكامل لدائرة منظم جهد متردد مبنية على معالج أصغر. منظم الجهد المقترح يعمل بطريقة التقطيع ولذلك يعطي تحسينات في الأداء يمكن أن توصف بما يلي:

ا) نطاق التحكم غير متعلق بزاوية الحمل.

ب) توجد علاقة خطية بين نسبة الوقت مع قيمة المركبة الأساسية من الجهد الناتج.

جـ) يمكن التحكم برتبة توافقيات جهد الحمل المهيمنة عن طريق تغيير تردد التقطيع.

المعالج الأصغر من نوع ز ـ ٨٠ يستخدم في تصميم التحكم. تخطيط البرامج المستخدمة إضافة إلى مكونات النظام موضحة. عرضت النتائج المعملية وما يتعلق بها من نظرية والمتعلقة بأداء المنظم مع أحمال خاملة. إضافة إلى ذلك عرضت مقارنة مع نظام التحكم بزاوية الطور لتوضيح مزايا النظام المقترح.