

ELECTRICAL ENGINEERING

A Very High Bandwidth Data Capture Interface for Microprocessor-Based Polarity Correlator

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Abstract. A microprocessor-based polarity correlator can be used as an alternative to the expensive MALVERN photon correlator in laser optical systems for low velocity measurement using cross-correlation.

In this paper a new very high data capture interface for the original polarity correlator which is built around Z-80 microprocessor is designed and implemented to cope with higher velocity measurements where a very high speed logging is required. The correlator is tested using artificial data, it shows a significant increase in the data logging speed by more than ten times.

Introduction

The only way of measuring the solids flow velocity in pneumatic conveying is by cross-correlation. The principle is to measure the time of flight of the flow between two axially spaced transducers sensitive to random flow irregularities. This technique does not cause flow obstruction besides its simplicity and reliability. The significant disadvantage is the cross-correlation calculation which requires quite elaborate and very expensive processing system.

One of the best techniques used to measure the flow velocity using cross-correlation is the two beam laser optical system. In this method, the tagging signals located along the flow axis are detected by an optical transducer when the variation in the intensity of light reflected by the passing particles. This gives a very high spatial resolution and covers a wide range of flow velocities besides its simplicity, but the data processing is very costly. The MALVERN correlator is widely used to compute the correlation function for such measurement. It is a digital photon correlator. Its prin-

ciple is to implement the correlation function by performing a series of shifts and multiplications using a sophisticated digital circuits.

A low cost high bandwidth microprocessor-based polarity correlator has been developed and built around Z-80 system to be used as an alternative [1] to the expensive MALVERN correlator to process the data received from laser optical system for low velocity measurement. The microprocessor task is to capture the data received from the up and down stream transducers in a form of zerocrossing instants and store them in two arrays in RAM. The computation of the cross-correlation function is performed when a predetermined number of zerocrossings has been logged. The data logging is performed using a special data capture interface which mainly consists of two direct memory access controllers (DMA), each DMA is responsible for one channel transfer which reads a real time clock then stores the reading in the corresponding array when a zerocrossing is received. A Z-80 counter timer circuit (CTC) is used for this timing.

The above design is quite satisfactory in applications where the velocity measured is fairly low, but in higher velocity measurements the data bandwidth gets higher which leads to the possibility of missing some of the zerocrossings of the logged signals which become very likely when the zerocrossings for both channels occur simultaneously. When this happens it is disastrous because missing just one zerocrossing causes cross-correlogram inversion.

This proposed work deals with a design of a novel very high data capture interface capable of logging very high bandwidth signals without missing any zerocrossing.

Zerocrossing Polarity Correlation

The data for the polarity correlation algorithm is sampled as a series of one bit samples and information is stored in memory in very long strings of zeros and ones particularly when data is oversampled for better resolution achievement as shown in Fig. 1a. A more efficient way of managing the data is to detect only the zerocrossing instants as shown in Fig. 1b, *i.e.* the only instants at which the signals change from zero to one and vice versa. The major advantage of such technique is the items to be handled are less and do not increase with increasing the sampling rate, because the number of zerocrossings is completely independent of the sampling rate. Therefore, the cross-correlation between the two channels is implemented directly from data in a form of zerocrossing times which are logged using a special data capture interface. As shown in Fig. 2 the two signals tend to spend a certain time together in agreement (both positive or negative) or disagreement (one positive and one negative), the

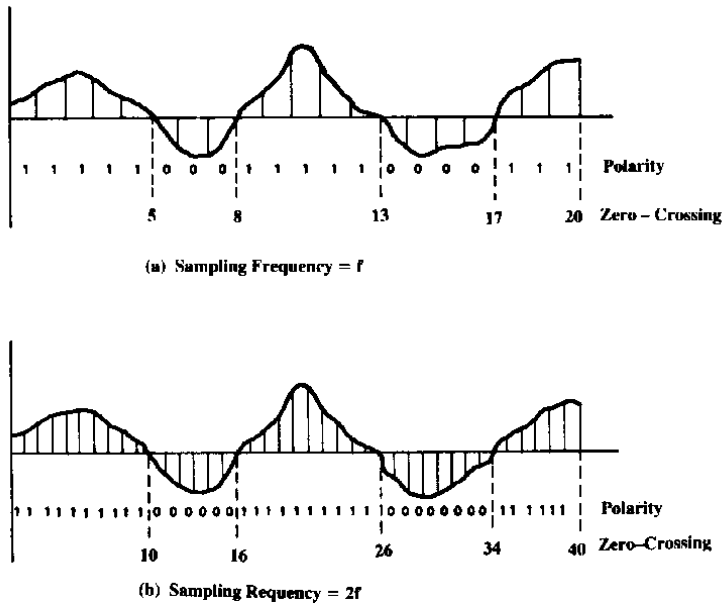


Fig. 1. Data coding by polarity and zero-crossing techniques.

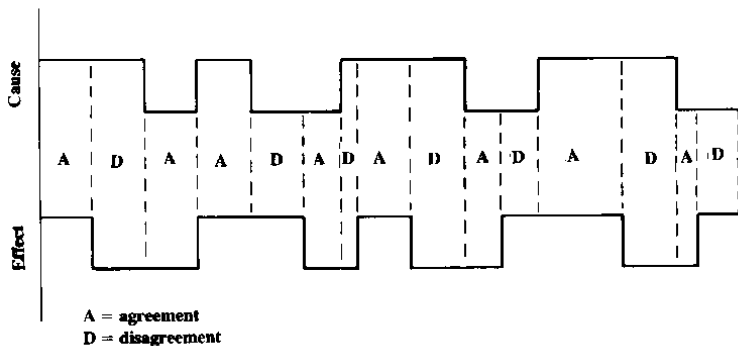


Fig. 2. CAUSE and EFFECT blocks of zero-crossing intervals.

cross-correlation is equal to the net agreement over the given observation period. One signal is shifted one clock period step to get the rest of the cross-correlogram points. By this algorithm the multiplication which consumes a lot of time is replaced by addition and subtraction.

Zerocrossing Extraction from Optical Data [2]

In the flow measurement using two laser beams the optical transducers consist of photomultipliers which detect the light scattered by passing particles then convert it to electrical signals in a form of spikes. Such signals can not be readily correlated and a special interface is required to change them to more managable forms. The simplified circuit layout is shown in Fig. 3, a time window is defined and the number of spikes received within any time window will be high if a particle is in the laser beam or low due to the background illumination if there is no particle.

Discrimination between the two conditions is on the basis of a threshold value set by a thumbwheel switch. The number of spikes received during each time window is counted and compared with the threshold value to give an output signal which can be correlated.

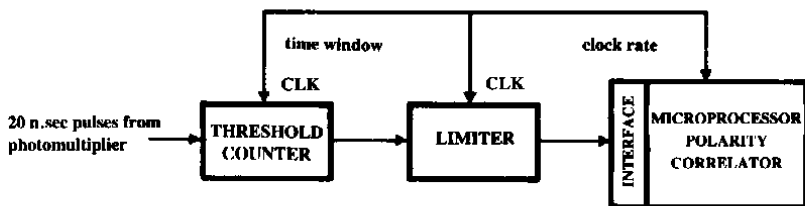


Fig. 3. The simplified circuit layout of the optical interface.

Microprocessor-Based Correlator

A high bandwidth low cost microprocessor-based correlator has been developed and built around Z-80 system [2]. The microprocessor mainly does two tasks:

- i) Reads the zerocrossing instants of both two channels received from the up and down stream transducers, and stores them in two arrays called CAUSE and EFFECT.

- ii) It will compute the cross-correlation function using a special assembly language program after enough predetermined data zerocrossing instants have been logged for both channels. The speed of computation depends totally on the execution time of the program and the number of zerocrossings required to be processed, while the data logging speed depends upon the technique used to implement the data capture interface which is discussed in the next section.

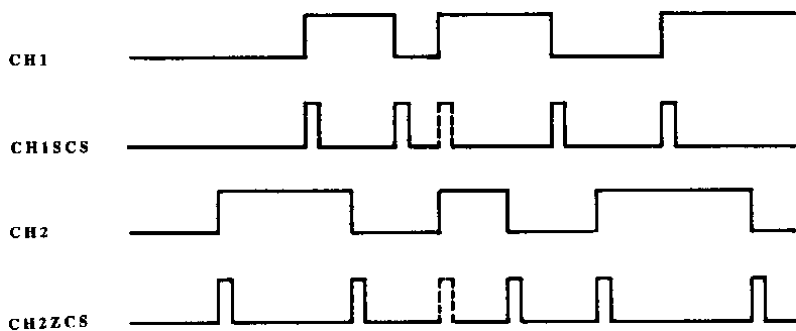
Data Capture Interface and Logging Speed

The data capture interface is two identical channels and each one mainly consists of a DMA for data transfer and a CTC as a real time clock. The DMA reads the CTC counter value and stores it in the corresponding block in memory when the zerocrossing arrives. To enable parallel transfer of both channels the DMAs are configured in single byte transfer where the system busses are only requested and acknowledged for single byte transfer when the DMA RDY input is triggered by the zerocrossing edge (either rising or falling) and the other DMA will not be served during this transfer which means that its zerocrossing will be missed, because the system busses are only devoted for the transferring channel.

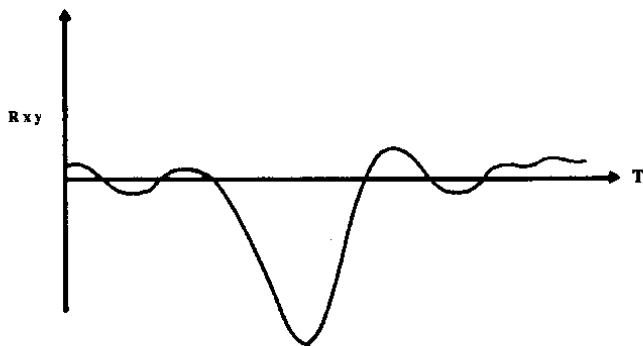
The busses are released after each single byte transfer has been done to give the chance for another zerocrossing to be logged from any channel. The single byte transfer in this mode and with Z-80 standard timing normally takes about 12 clock cycles, four cycles for read, three cycles for write, two cycles for busses stealing, two cycles for busses release and one cycle for RDY input activation. So the maximum data logging can be achieved using such configuration with a 4 MHz clock is equal to the maximum transfer rate of both DMA's in parallel which is found experimentally to be 130,000 zerocrossing/sec. The design as mentioned above has some disadvantages which become significant on higher velocity measurement applications where the signals bandwidth becomes very high, the disadvantages are:

- 1) The data logging speed is limited for higher velocity measurements.
- 2) When the zerocrossings from both channels occur at the same time one of them will be ignored as shown in Fig. 4a. This will lead to a cross-correlogram inversion. See the inverted cross-correlogram Fig. 4b.

These two major disadvantages are overcome by a modified design. In this design both DMA's are configured in different mode. The whole new interface design is explained in the following section.



a) Timing diagram of the zerocrossing detection.



b) Inverted crosscorrelogram.

Fig. 4. a) Timing diagram of the zerocrossing detection.
b) Inverted crosscorrelogram.

The New Data Capture Interface

The old design is modified by configuring both DMA's in continuous mode, in this mode the DMA will not release the system busses until the predetermined block has been transferred when the DMA is enabled to gain the system busses. The transfer rate of such configuration is very fast compared with the previous one, only three cycles are required, two for reading and one for writing, when the DMA unique feature of varying the cycle time is used. The data logging speed becomes 1.330.000

zerocrossing/sec, and due to using this configuration the possibility of missing any zerocrossing no longer exists.

The data capture interface is divided into two sections for channel one and two data transfers. Each section mainly consists of a zerocrossing detector which detects both positive and negative transition instants of the received signals from the optical data interface. The DMA is activated by the output of the zerocrossing detector which is in the form of a train of pulses with widths equal to one system clock period. These pulses are fed to the RDY input of the DMA which in turn reads the CTC reading and stores it in the corresponding array in memory whenever a zerocrossing is received.

As shown in Fig. 5 the zerocrossing detector consists of two monostable multivibrators (MMV) which generate a pulse whenever the signal changes state either rising (+) or falling (-). A flipflop is used to let the first zerocrossing detected is in a known sense for both channels (say +), otherwise the cross-correlogram peak might be inverted as discussed earlier.

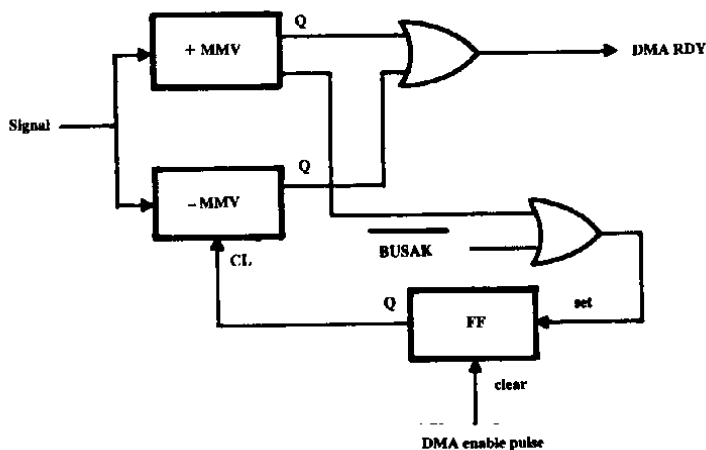


Fig. 5. Zerocrossing detector circuit.

At the start of logging the flipflop is reset to disable zerocrossings of the negative transition using the DMA enable pulse. These negative zerocrossings are reenabled when the first positive transition has been logged.

There are three major problems which will arise when DMA's are configured in continuous mode for parallel transfer of both channels. These problems are:

- i) When the DMA's are both used in the continuous mode each one is considered as an independent processor which generates its own control and timing signals during its block transfer. So each DMA, its CTC, and the storing RAM chip with the associated busses must be isolated during the transfer.
- ii) The two DMA's must be enabled to gain the busses simultaneously, otherwise the CPU busses will be tristated just after the first DMA being enabled thus preventing the other one from doing so.
- iii) The cross-correlation function is implemented as described earlier by cross-correlating the zero-crossing instants of both channels. This requires that both channels should be based on one timing clock.

These problems mentioned above are overcome by the design shown in Fig. 6. Each DMA has its own CTC and 2k RAM chip which are isolated from the other one during the transfer to prevent the transfer overlapping which will occur between the two channels. The address and control busses are unidirectional where the flow direction is out of the CPU and are tristated by the BUSAK pulse when both DMA's are enabled for data transfer. While the data bus is tristated at the same manner,

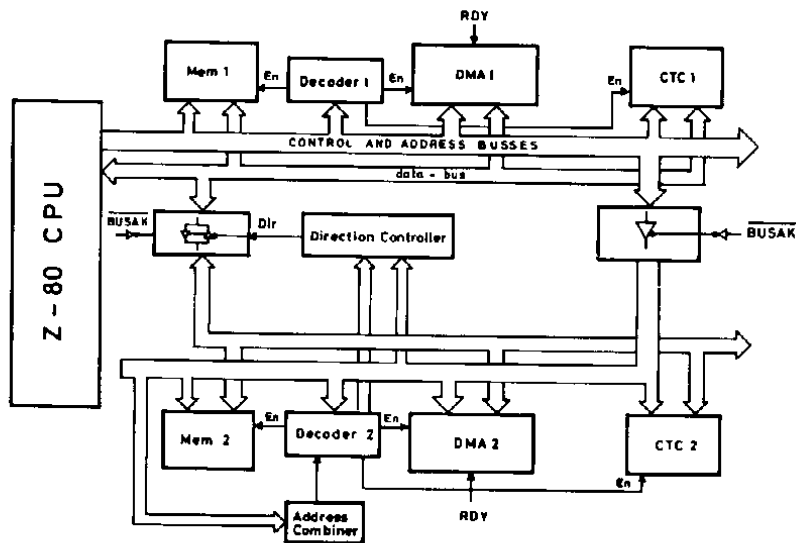


Fig. 6. The new data capture interface.

because it is a bidirectional bus the data flow when the transfer is disabled is from the CPU to the logging interface except in the following conditions:

- i) The DMA status register is read.
- ii) The CTC channel is read.
- iii) The RAM chip is read.
- iv) The interrupt is acknowledged, because in the Z-80 interrupt mode 2 the lower byte of the interrupt vector is supplied by the interrupting device when the interrupt is acknowledged by the CPU. The acknowledging signal is formed by OR gating the MI and IORQ signals.

In Fig. 7, the DMA chip is configured by sending a number of control words to its port which is decoded to a specific address. The last control word sent is the DMA enable one. The two DMA's can be only enabled simultaneously by sending the enable control word for the corresponding port addresses at the same time. To do so, one of the ports address is decoded. One of the DMA's port address is decoded by software to have the same address of the other DMA port temporary during only sending the enable control word to both DMA's at the same time. The third problem mentioned earlier is that the CTC is configured in such application by sending one control word followed by a time constant been sent. This means that a time delay between the two CTC chip will appear due to the software configuration. This delay will cause an offset value to the cross-correlogram. To get around this problem both CTC chips are interfaced with the CPU at the same port address which makes both CTCs start counting simultaneously. Using one port address for both CTCs will not cause data overlapping because the CTCs are utilized only during data logging where the two channels will be isolated.

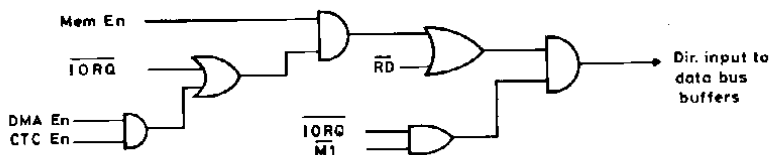


Fig. 7. The data bus direction controller.

Results

The microprocessor-based correlator with its very high bandwidth data logging interface is built around very low cost microprocessor kit (MPF-IP microprocessor). The tests carried out on some artificial very high bandwidth data produced from a random signal generator shown in the photograph Fig. 8 with a clock period 3.33 μ sec.

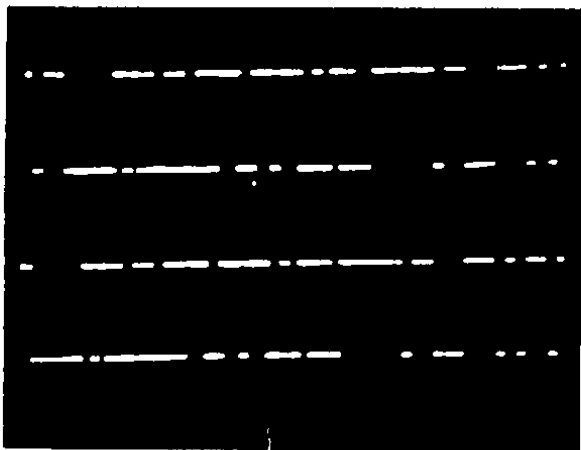


Fig. 8. Photograph of random signal generator output of clock period = $3.33 \mu\text{sec}$.

The photographs shown in Fig. 9 show the cross-correlogram of the delayed random signals. Fig. 10 shows the cross-correlogram of different time delay. The continuous on-line non inverted cross-correlograms prove that missing any zerocrossing no longer exists in both input channels logged. This also can be checked by checking both CAUSE and EFFECT arrays located in RAM's.

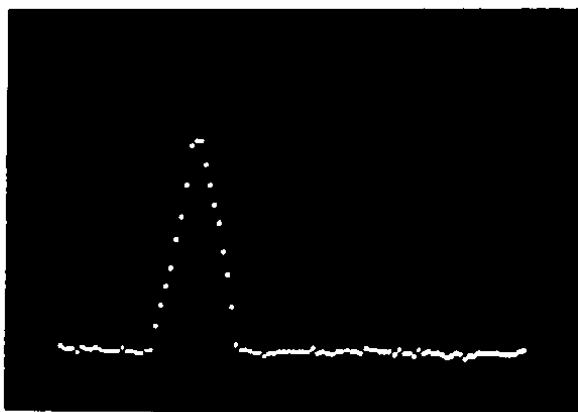


Fig. 9. Photograph showing the cross-correlogram of two delayed random signals.

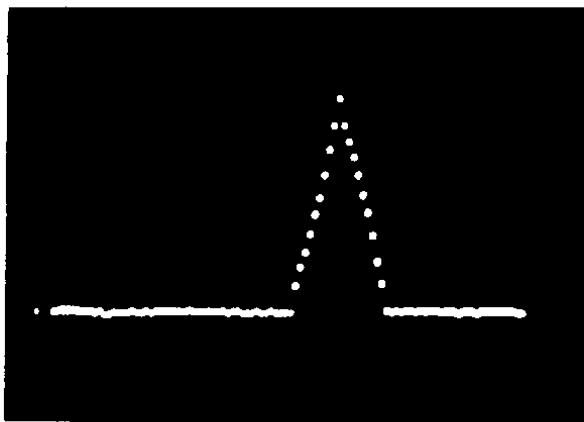


Fig. 10. Photograph of cross-correlogram for different time delay.

Conclusions

This paper shows that the microprocessor-based polarity correlator with its modified data capture interface has a very high data logging speed which is about 1.330.000 zerocrossings/second (more than ten times faster than the old design) without missing any zero crossings. This makes very low cost correlator to be a very good alternative to the expensive MALVERN correlator in high velocity measurements. This will reduce the price to more than one-tenth that of MALVERN correlator. This work can be extended to speed up the cross-correlation computation time.

References

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دائرة تقابل التقاط البيانات ذات النطاق الترددي العالي جدا للرابط القطبي

المعتمد على المعالج الدقيق

عبدالله محمد السويلم

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ملخص البحث. إن بالإمكان استخدام الرابط القطبي كبديل للربط الفوتوني (مالفرن) عالي التكلفة في أنظمة الليزر البصرية لقياس السرعات البطيئة باستخدام الترابط التقاطعي.

هذا البحث عبارة عن تصميم وبناء دائرة تقابل للتقاط البيانات ذات النطاق الترددي العالي جداً للرابط القطبي المبني باستخدام المعالج الدقيق ز- ٨٠ وذلك لقياس السرعات العالية والتي تتطلب سرعة عالية في التقاط البيانات. جُرب هذا الرابط باستخدام البيانات الصناعية وأثبت سرعة متميزة في التقاط البيانات تفوق العشرة أضعاف.